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Design of a Multi-channel Data Acquisition and Storage Device Based on FPGA

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Abstract: With the rapid development of aerospace, missile launch, satellite navigation and other fields, more and more signals need to be collected and stored in various research and application. The parameter performance of each load on the detector is of great significance to the detector performance evaluation and structure optimization. In these fields, data acquisition and storage systems are mainly used to collect and store various sensor data in the work of flight devices, such as pressure signal, image signal, temperature signal and other key data. The recording of these data has an important reference value for the next experimental improvement.

1. Introduction

This paper introduces a data acquisition and storage device based on the field programmable gate array (FPGA), which can realize the real-time acquisition, conversion, storage and transmission of multiplex signals. With the high-performance AD conversion chip and the high-speed processing capability of FPGA, the real-time acquisition, conversion, frame editing and data storage of multi-channel data are realized. At the same time, communication and external telemetry are realized through Gigabit Ethernet. The experiment proves that the device can meet the requirements of high-speed, real-time and multi-channel signal data acquisition and storage.

2. Advantage and application of FPGA in data acquisition

FPGA has many advantages in data acquisition and has been widely used in various fields.

2.1. Multi-channel data processing

FPGA has rich I / O interface and parallel computing capabilities, which can realize the simultaneous processing of multi-channel data and improve the efficiency of data collection.

2.2. High-speed data acquisition

FPGA integrates high-speed AD converter and other modules internally, which can realize high-speed data acquisition and conversion, and is suitable for the processing of high-frequency signals.

2.3. Flexibility and programmability

FPGA can be flexibly programmed according to specific data processing requirements to realize customized data processing algorithm.

2.4. Low power consumption

Compared to traditional processors, FPGA has lower power consumption, which helps to reduce the energy consumption of the system.

Some typical application cases of FPGA in data collection include satellite data processing in the space field, biomedical data collection and analysis in the medical field, and sensor data acquisition in industrial automation, etc[1].

3. Design principle and overall architecture of multi-channel data acquisition and storage device based on FPGA

3.1. Design principle

The design principles proposed in this paper mainly include AD conversion chip, FIFO, dual-port RAM, FPGA master control module, GPIO interface and Gigabit Ethernet module.

3.1.1. AD conversion chip

The AD7606 chip is used as the AD conversion chip. The AD760 is a high-speed, low-power 16-bit AD converter with eight analog input channels and a maximum sampling frequency of up to 200 kHz.

3.1.2. FIFO

FIFO (First in First Out) is a first-in, first-out data cache used to cache AD converted data. FIFO generated inside FPGA was used with each FIFO capacity of 4K.

3.1.3 Dual-port RAM

Dual-port RAM is a RAM with two separate ports for caching data in a FIFO. Two 8K dual-port RAM were used, with each RAM divided into 4 zones, each being 2K.

3.1.4 FPGA master control module

FPGA master control module is the core of the system and is responsible for controlling the operation of each functional module. The main functions of the FPGA master control module include: detecting and responding to external trigger signals, controlling the tasks module performing the task; receiving and analyzing instructions from the experimental process control module through the GPIO interface; collecting the 16-channel analog quantity signal and the acquired data in the external FLASH memory in addition to SRAM[2].

3.1.5 GPIO interface

The GPIO (General Purpose Input Output) interface is used to realize the communication between the FPGA and other devices. The communication between the FPGA and the experimental process control module is realized through the GPIO interface.

3.1.6 Gigabit Ethernet module

Gigabit Ethernet module is used to realize the communication and external telemetry between FPGA and the upper computer. Gigabit Ethernet PHY and network transformer interface are used to realize network communication.

3.2. Overall structure

The overall architecture designed in this paper mainly includes multi-channel analog signal acquisition, AD conversion, FPGA master module, storage and transmission.

3.2.1. Multi-channel analog signal acquisition

The device collects multi-channel analog signals through sensors and other devices, including 16-channel analog volume signals, 7-channel switching volume signals and LVDS signal of the test product.

3.2.2. AD conversion

The device transforms the collected analog signal through the AD conversion chip to convert the analog signal into a digital signal.

3.2.3. FPGA master module

The FPGA master module receives the AD converted data and processes it. The main functions of FPGA master control module include: caching the data after AD conversion; controlling the frame compilation and storage of data; receiving and resolving instructions from the experimental process control module through the GPIO interface; and realizing communication and external telemetry through the Gigabit Ethernet interface.

3.2.4. Storage and transmission

The processed data is stored in the external FLASH memory and transmitted to the upper computer in real time through the gigabit Ethernet interface.

4. Hardware design details

4.1. AD7606 chip selection and its characteristics

The analog signal acquisition module adopts AD7606 chip, which is a high performance, low power 16-bit successive approximation ADC. The AD7606 chip has eight simulated input channels, each with an independent sampling retention function. Its maximum sampling frequency can reach 200 kHz, which meets the requirement of simultaneous sampling of multi-channel analog signals. In addition, the AD7606 chip has built-in analog input bit protection, second-order anti-aliasing filter, tracking holding amplifier and other circuits, which simplifies the design of external circuits and improves the reliability of the system[3].

4.2. Timing design of FPGA control AD7606

FPGA enables real-time acquisition of multi-channel analog signals by controlling the sampling retention, conversion and data read timing of AD7606. During the design, FPGA receives external trigger signals through the GPIO interface and controls the sampling holding circuit of AD7606 for

synchronous sampling. After sampling, the FPGA controls the conversion circuit of the AD7606 for data conversion and reads the converted data inside the FPGA for processing. FPGA realizes the real-time acquisition of multi-channel analog signals, which ensures the accuracy and reliability of data acquisition.

4.3. Receiving and storage of LVDS transmission signals

The FPGA also receives the LVDS transmission signal from the external products and stores it in the FLASH memory. LVDS (Low Voltage Differential Signaling) is a high-speed, low-power serial data transmission technology. Through the LVDS receiver integrated within FPGA, the reception and synchronous disconnection of LVDS transmission signals are realized. The disconnected data is stored in the FIFO (First In First Out) cache inside the FPGA, and then framed and stored through the dual-port RAM. The LVDS transmission technology enables real-time reception and storage of high-speed serial data.

4.4. FLASH memory selection and read and write speed test

The data storage module uses the MT29F32G08 FLASH chip produced by Micron Corporation as the storage medium. The chip has 4GBytes of memory, and can perform 60,000 programming and erase operations at operating temperatures of-40℃ to 85℃. The MT29F32G08 chip adopts an asynchronous NAND interface to transmit data through parallel data lines with FPGA. In terms of read and write speed, the read and write speed of the chip is 4 MB/s, which meets the demand for high-speed data storage. The FLASH memory showed good stability and reliability in the experiments[4].

4.5. Design of power supply circuit and interface circuit

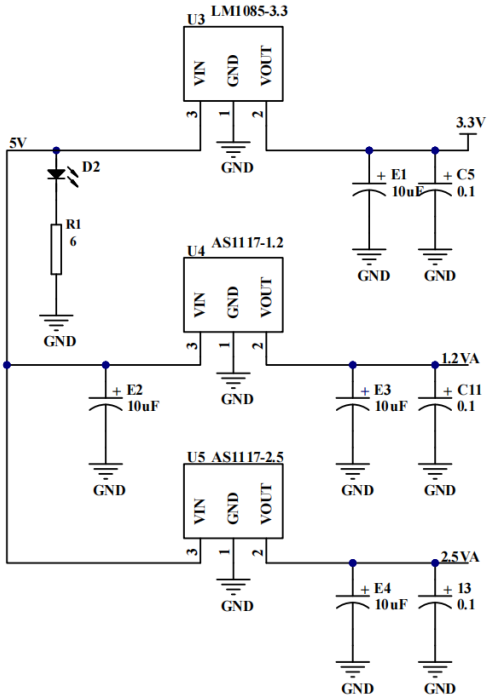

Figure 1: FPGA power conversion circuit

The power supply circuit design adopts power supply chips such as AS1117-2.5, AS1117-1.2

and LM1085-3.3 to convert the 5V input power supply into different voltage levels such as 3.3V,2.5V and 1.2V, meeting the power supply requirements of chips such as FPGA, AD7606 and LVDS receivers. The interface circuit design includes the network interface and the GPIO interface to realize the communication and control of FPGA with other modules. The network interface adopts Gigabit Ethernet PHY and network transformer to realize the data transmission between the upper computer. The GPIO interface is used to receive external trigger signals and send control signals to realize the control of the AD7606 and LVDS receivers. As shown in Figure 1.

5. Software design details

5.1. Data read and write logic of FIFO and dual-port RAM

The data storage logical design includes data caching and storage operations for FIFO and dual-port RAM. The FIFO (First In First Out) cache unit enables the caching and temporary storage of different types of data signals. Each FIFO has a capacity of 4K, and a total of five FIFOs were generated for storing different types of data. When the data stored by FIFO is half-full, or 2K, the data is read from FIFO into the dual-port RAM. Each RAM has a capacity of 8K, divided into four zones, 2K each, and a total of two RAM. When the data in each zone reaches 2K, the data is read from the output port of the RAM and stored in the FLASH. The design of data reading and writing logic ensures the order and timeliness of data.

5.2. Data processing logic of the FPGA main control module

The FPGA master control module is the core of the whole system and is responsible for controlling and coordinating the operation of each functional module. The main functions of the master control module include detecting and responding to external trigger signals, controlling each functional module to perform tasks, receiving and analyzing instructions from the experimental process control module, and collecting analog quantity signals, switch signals and LVDS signals. The master control module interacts with other modules through the GPIO interface, transmits the collected data in real time, and stores the data into FLASH. The main control module communicates with the upper computer through the Gigabit Ethernet port, and transmits the test product status parameters and analog data. Through the reasonable data processing logic, the master control module realizes the functions of data collection, storage and transmission.

5.3. Data framing and transmission logic

Table 1: Ethernet communication frame lattice

order number	field	Byte number	content
1	Frame	2byte	0xFC 0x61
2	head	4byte	Frame-head-to-frame-tail length
	DL	1byte	
3	data type	9byte	Experimental parameters
4	Date, time		Year is 2 bytes, month 1 byte, day 1 byte, unsigned integer.
...	data		Pilot area data
n	sum check	1byte	Excluding sum check and frame tail, all bytes are added with no carry 0x21
n+1	Frame tail	1byte	

Data frame editing and transmission logic is the key part to ensure the accuracy and integrity of data transmission. After the data acquisition device processes and stores the collected data through FPGA, the data is sent to the telemetry device by data frame mode. The format of the data frame includes the information header and several information words, and the data is sent in the specified content order. If one parameter in the message content occupies multiple bytes, it is sent in the order of the next. After the frame processing of FPGA, the data is sent to the telemetry device in real time through the Gigabit Ethernet port, which realizes the rapid transmission and real-time monitoring of the data. The specific communication frame format is shown in Table 1.

5.4. Data read-back logic and file generation

At the end of the experiment, it is necessary to read back and distinguish all kinds of data stored in the total control storage unit. According to the test situation, the data will automatically select the data block number that needs to be read back for read operation[5]. After reading, the data automatically parses and generates a folder containing all kinds of data. Through this data readback logic and file generation method, the convenient access and management of the data stored in FLASH is realized.

6. Experimental testing and result analysis

6.1. Power supply performance test: output voltage and ripple test

In the power supply performance test, the digital multimeter and the oscilloscope are mainly used to measure the actual voltage and ripple of the output power supply of each power supply module. The results show that the error value of each output voltage of the system power module of the system does not exceed 2%, and the peak ripple is less than 30 mV, which fully meets the power supply requirements. This shows that the power supply module performs well and can provide a stable power supply for the system. See Table 2 for details.

Table 2: Power supply test values

Power type	Expected voltage value / V	Actual voltage value / V	Voltage value error /%	Peak ripple rate / mV
VCC24	+24	+24.05	0.21	23.5
VCC12	+12	+11.95	0.42	16.3
VCC5	+5	+5.02	0.40	14.1
VCC3.3	+3.3	+3.32	0.61	15.1
VCC2.5	+2.5	+2.514	0.56	13.7
VCC1.2	+1.2	+1.198	0.17	12.1

6.2. Data acquisition function test: real-time performance, accuracy and storage capacity test

As shown in Table 3, in the data acquisition function test, the total amount of data collected per second during the experiment was first calculated, at about 3.17 MB/s. The data storage period is 10 seconds, and the total amount of data stored in a single experiment is about 32MB. The 4GB capacity of FLASH theoretically supports the storage requirement of no less than 100 experiments.

The final data shows the stored two pressure sensors and the three-phase current value data. The red box is the resolved time mark, indicating that the time period of data storage is 10ms, and the blue box is the corrected value of the pressure sensor. This proves that the system has good real-time performance, accuracy and storage capability.

Table 3: Real-time storage of data volume statistics

data source	number of channels	Sampling rate (port rate)	Data volume (KB/s)
Analog volume data	16	1Ksps	32
Switch volume data LVDS data Motor status data	7	1Ksps	7
	1	25Msps	3125
	1	48Ksps	6
	amount to		3170

6.3. Comparative analysis of experimental results and expected results

By comparing the analysis of the experimental results with the expected results, we can see that the system fully meets the design requirements. The experimental results prove that the system has good performance in power supply performance, data acquisition function and other aspects, which meets the needs of practical application. This shows that the design of the system is successful and can provide effective solutions for data acquisition in space exploration, missile launch and other fields.

6.4. Field test and application effect evaluation

In field tests, the system was applied to practical detection tasks, where various load parameters on the detector were collected and stored in real time. Through field testing, we found that the system can collect various load parameters accurately and in real time and store them in FLASH. During the test process, the system showed good stability and reliability to meet the needs of practical application. This proves that the system has a good application effect and can provide effective data support for actual detection tasks.

7. Conclusion

The multi-channel data acquisition and storage device based on FPGA designed here showed a good performance in the experimental test. Through power performance test, data acquisition function test and field test, we prove that the system has good performance in terms of power stability, real-time data acquisition, accuracy and storage ability. This provides strong support for practical application, proving that the design of the system is successful and has high practical value.

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