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# *Hardware Implementation of Artificial Synapses*

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***Abstract:*** The simple two-terminal metal-insulator-metal (MIM) structures of memristors make them capable of being integrated into dense crossbar arrays [1, 2]. As shown in Figure 1, a typical crossbar array consists of parallel metal lines, termed word lines and bit lines, respectively, as the top and bottom electrodes that are perpendicular to each other. The bidirectional memory is connected between the word line and the bit line. During the read process, the extra current generated by the natural path represented by the red solid line can reduce the energy consumption of the unselected unit, thus reducing the read mosaic and limiting the size of the array. In order to independently control the read/write operations of each memory unit in the array, the 1T1R structure is proposed.

## 1. Introduction

Developmental memory is composed of word lines and bit cells. During the read process, the current of the red solid line path represented is not welcomed, which will lead to extra unselected cell loss, thus reducing the read gain rate and limiting the array size. In order to independently control the write/read operations of each memory in the crossbar array, many 1T1R structures have been proposed. Since a memory can only represent positive discrete weights, CMOS developmental hybrid memory technology can achieve complete symmetric programming, which traditional arrays cannot achieve. This mouse architecture is connected with the built-in memristor array computing characteristics to realize massive parallel computing, greatly improving the speed of grey computing. So far, a lot of research has been done to discover the partition flow of RRAM, PCM, CBRAM and other arrays. These platforms include cell engineering, such as accessing elements input to a single memristor (1R) to create complex cells, such as transistor-one memristor (1T1R), diode-one memristor (1D1R), selector-one memristor (1S1R), self-correcting memristor, etc. [4-6] The introduction of the access device not only improves energy efficiency during array programming, but may also assist memristors in implementing synaptic plasticity, thus enabling novel analog machine learning and neuromorphic computing.

## 2. Sneak Path Problem

The simple two-terminal metal-insulator-metal (MIM) structures of memristors make them capable of being integrated into dense crossbar arrays [1-3]. As illustrated in Figure 1, the crossbar array is composed of parallel metal lines, referred to as word lines and bit lines, which intersect each other. At the intersection of the word lines and bit lines, two-terminal memristors are formed. During

the read process, the contact path represented by the dashed line transmits an unnecessary current, leading to additional energy loss of the unselected cells, which consequently reduces the read margin and limits the size of the matrix. To independently control the write/read operations of each memristor in the crossbar array, many 1T1R matrix structures have been proposed. Taking into account that memristors can only provide digital support, these structures are essential for nature and science. The CMOS-Memristor hybrid technology can completely parallel programming operations, while traditional Crossbar arrays cannot. Combined with the built-in Memristor array operations, these Crossbar arrays can realize large-scale signal transmission parallel processes, which can significantly improve the extraction speed compared with the serial extraction method. So far, a lot of research has been done, focusing on the coverage current of RRAM, PCM, CBRAM and other arrays. These sequences have retained the construction of a single client, such as the access entrance of a 1-Memristor (1R) element, to create a composite client, such as 1T1R, 1D1R, 1S1R, self-feedback Memristors, etc. [4-6] The introduction of the access device not only improves energy efficiency during array programming, but may also assist memristors in implementing synaptic plasticity, thus enabling novel analog machine learning and neuromorphic computing.

### 2.1. Memory Unit Cells

In this paper, we have outlined a variety of materials or structures that have been demonstrated in recent years for memory array, in order to realize the expectation of next-generation hardware storage. Specifically, we provide a comprehensive overview of memory cells for addressing the synaptic current problem, including 1S1R, 1T1R, 1D1R, Selective Storage (SSC), Self-Calibrated Storage (SRC) and Compensated Controllable Reversal Storage (CRS), as shown in Figure 2. Furthermore, we also provide a comprehensive overview of memory cells for addressing the synaptic current problem, including 1S1R, 1T1R, 1D1R, Selective Storage (SSC), Self-Calibrated Storage (SRC) and Compensated Controllable Reversal Storage (CRS), as illustrated in Figure 2.

### 2.2. Bias Schemes

In order to reduce programming complexity, various lock configurations, as illustrated in Figure 2, are proposed to lock the selected cell voltage of the unselected cells. Regardless of the source of the memristor current/conductance "off" between the two poles, selecting a lock configuration to perform the write/read process can help reduce the underload current issue. According to the voltage on the unselected bits and word lines when the selected cell is completely locked, the voltage can be classified. The flow configuration puts all unselected words and bit lines in a flowing state. The read margin of the flow configuration may be significantly lower than that of the 1/2V configuration, because if it cannot be sufficiently suppressed, the underload current of all unselected cells will flow into the V voltage, thus leading to a decrease in read margin. Compared to other types, RRAMs have higher reliability, larger capacity, and can operate at low voltages, as well as at 0V. In the second type of reliability at 1/2V, the memory can be triggered and can operate at low voltages, as well as at 0V (three types). Subsequently, in the second type of reliability at 1/3V, the memory can be triggered and can operate at low voltages, as well as at 0V. Furthermore, RRAMs are capable of operating at a wide range of voltages, from 0V to 1/2V and 1/3V, making them suitable for a variety of applications.

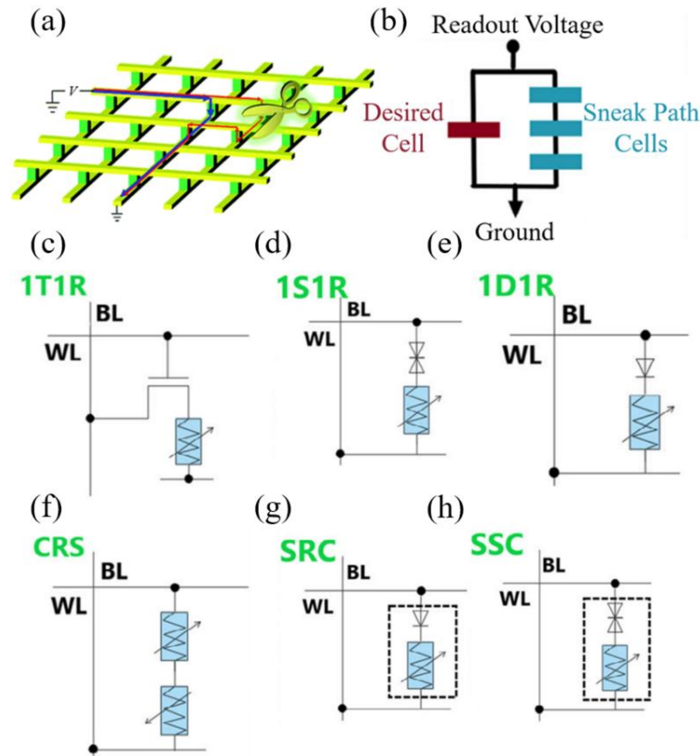


Figure 1: (a) Schematic illustration of crossbar memory array architecture, with normal and sneak current paths, respectively [5]. (b) The equivalent electric circuit of sneak current is involved in the crossbar array. Six types of possible solutions to solve the sneak-path current issue, including (c) 1T1R, (d) 1S1R, (e) 1D1R, (f) CRS, (g) SRC, (h) SSC.

## 2.3. S1R Cells

The 1S1R element is a two-terminal scheme composed of a single selector and a single series memory, which is considered to be the most suitable for high-efficiency 3D integration RRAM [6]. It has a large non-linearity of I-V characteristics, as well as a low threshold voltage and memory voltage variation. Furthermore, the selectors must be compatible with the memory in terms of working current and voltage range in order to provide a limited access current of the non-selected memory elements during read and write operations, thus avoiding interference with the memory work and ensuring high reliability with cyclic power, matrix scale and chip variability. Compared to single-channel components and transistors, which are very difficult to stack vertically and thus have limited final integration, the selector is actually a large two-channel non-linear resistor and offers interesting prospects for high-efficiency integration. The 1S1R element has the advantage of being able to provide a high degree of integration, as well as a low power consumption and a high degree of reliability. Moreover, its non-linearity of I-V characteristics and low threshold voltage and memory voltage variation make it an ideal choice for 3D integration RRAM applications. Additionally, the selectors must be compatible with the memory in terms of working current and voltage range in order to provide a limited access current of the non-selected memory elements during read and write operations, thus avoiding interference with the memory work and ensuring high reliability with cyclic power, matrix scale and chip variability. In conclusion, the 1S1R element is a promising solution for high-efficiency 3D integration RRAM due to its large non-linearity of I-V characteristics, low threshold voltage and memory voltage variation, as well as its compatibility with the memory in terms of working current and voltage range. Currently, various solid-state memory systems exhibiting selector functions have been intensively studied, such as silicon selectors, field-assisted superlinear

threshold selectors, and mixed ion-electron conductive selectors. Each of them has its own advantages and disadvantages, which have been thoroughly analyzed by Aluguri et al. A multifunctional control device with a simple Pt/$NbO_x$/TiN structure was created and shows excellent 1S1R characteristics and transition threshold properties, as shown in Figure 2, Aluguri, finite element analysis was used to analyze and further support the multifunctional features. A multifunctional device was demonstrated and the mechanisms of multifunctional features were analyzed to help drive the application of 3D storage technology, which was analyzed in detail by Chen et al. A 1S1R type CBRAM selector-memory was demonstrated using Cu/Ti/$HfO_2$/$TiO_2$/TiN materials. Depending on the thickness of the $HfO_2$ layer and the device operating conditions, it can simulate the 1S1R operation. By utilizing the finite element analysis, Aluguri et al. have demonstrated a multifunctional control device with a simple Pt/$NbO_x$/TiN structure, which exhibits excellent 1S1R characteristics and transition threshold properties. Furthermore, Chen et al. have analyzed in detail the application of 3D storage technology by demonstrating a 1S1R type CBRAM selector-memory using Cu/Ti/$HfO_2$/$TiO_2$/TiN materials. The device can simulate the 1S1R operation depending on the thickness of the HfO2 layer and the device operating conditions.

The anatomy of the filament is controlled by using an ultra-high frequency flow shaping process at optimized high temperature. The conduction mechanism at sub-nA approach goes back to the jump with low energy 1 eV and jump at 0.7 nm distance. Compared to other reported works, the devices used in this work have the ability to show an ultra-high frequency flow current of 300 mA, can work with an ultra-high frequency power of 5 W, with a very high ratio of high compatibility/low compatibility $> 3 \times 10^3$ and high nonlinearity $> 3 \times 10^3$. After further optimization, the sub-quantum selector memristor without Cu/Ti/$HfO_2$/$TiO_2$/TiN construction will be useful for IoT devices discussed in detail by Hwang et al. The YSZ/Zr memristor with low form voltage (<1.5 V), low first current drop (150 μA), fast switching (2 ns), low voltage (<1 V) and current (50 μA) switching current, as well as abilities to multiple conduction states, will be reported, as shown in Figure 2. The low activation energy of the concentration windows (Ea, diffusion = 0.7 eV) measured in the switching ball YSZ enables the proposed memristor to have low-energy operation, which gives it better selection compatibility than most others. To demonstrate the proof principle, a vertically integrated circuit with a tunnel selector was successfully used for electroforming a memristor with a selector implemented in a self-built 1S1R device. Subsequently, 1S1R cells in a small array ($2 \times 2$) were investigated and the electroforming and switching operations demonstrated by Upadhyay et al. were shown. It was proposed and experimentally confirmed that the smoothness of the shell and the shape of the tunnel barrier play a decisive role in determining the nonlinearity of tunnel selectors. To prove the concepts, the research team developed the TLTB selector based on Ge/Pt/ $TaN_{1+x}$/$Ta_2O_5$/$TaN_{1+x}$/Pd, which combined the advantages of a potential barrier with smooth BE contacts. The proposed selector is CMOS compatible, can be built into a 3D stack, and shows a record NL. The measured RMS roughness and peak-to-valley height distribution were 185 and 700 pm, respectively. This ultra-smooth BE surface and peak barrier led to the demonstration of a record NL of $3 \times 10^5$. We then integrated the proposed TLTB selector vertically with a Pd/$Ta_2O_5$/Ru-based memristor device to demonstrate the integrability and 1S1R operations. The I–V characteristics recorded from this vertically integrated 1S1R cell showed a maximum on/off ratio of 100 and an NL of $10^4$, which is also a record NL of any vertically integrated 1S1R cell as discussed in detail by Upadhyay et al.

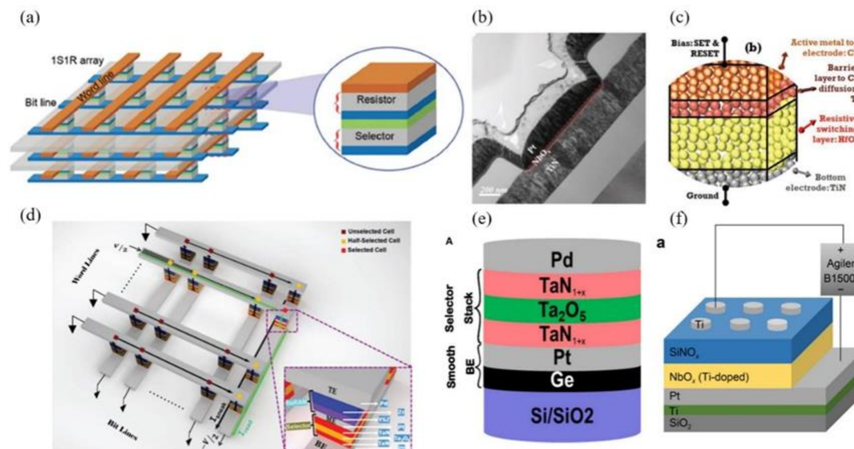


Figure 2: Typical 1S1R-based devices.

## 3. Conclusion

Based on the 1S1R cell, this study has demonstrated that the CTe resistance is mainly limited by a severe carbon segregation during switching. To address this issue, additives were introduced into the CTe system to improve the resistance while maintaining a low threshold voltage. Consequently, an optimal process was developed to achieve a selector device with a threshold voltage of around 1.3 V, a resistance >$10^{11}$ and an $I_{OFF}$ <5 nA. This work identified carbon segregation as the primary cause of resistance degradation in CTe selector devices. Wu et al. further elucidated that the stability of the amorphous CTe network can be enhanced by incorporating antimony-free elements. As illustrated in Figure 2, a $NbO_x$-based selector with added titanium was applied to a $SiNO_x$-based RRAM to form a 1S1R Pt/$NbO_x$ (Ti-doped)/$SiNO_x$/Ti cell, thereby suppressing the hidden path current. The resulting 1S1R exhibited a stable current resistance (>200 cycles), an adequate memory window (>40), a corresponding selectivity (>40) and a high uniformity of switching parameters. Moreover, the capacity of the 1S1R array was found to be approximately 1000 times larger than that of the RRAM. Furthermore, the absence of an intermediate metal in the 1S1R enabled its use in a 3D vertical RRAM cross-connection array, as described in detail in Yu et al.'s article. This work thus enabled the implementation of 1S1R memory applications with a high density of cross-connections.

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