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Multi-Channel High-Speed and High-Precision Signal Acquisition, Storage and Playback System

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Abstract: A multi-channel signal acquisition, storage and playback system with high speed and high accuracy is proposed by reprocessing the signals that can't be processed in real time and reproducing the collected signals in other places. Through FPGA control acquisition system, linear optocoupler is used to filter out high-frequency signal interference, ADS1258 realizes the conversion of 16 channels of analog data, asynchronous buffering technology buffers high-speed data, and sampling voting and delay filtering are combined to improve the stability of switch control instructions, and finally 16 channels of data are collected and stored.

1. Introduction

With the increasing demand for the detection of atmospheric composition and content, the Fourier transform spectrum detection technology based on interference has become the development hotspot of infrared spectrum detection technology at home and abroad because of its many advantages, such as large luminous flux, wide spectral range and high spectral resolution[1].

In the Fourier transform spectrum detection technology, the atmospheric infrared radiation signal has the characteristics of low signal amplitude, large dynamic range, and high detection accuracy requirements. It has high requirements on the anti-interference ability, noise suppression level, quantization digits, etc. of the detection system. At present, the research of weak signal detection mostly focuses on weak voltage signal detection, and some researches have analyzed the design of amplification circuit for weak voltage signal[2]. Some researches focus on the design of pA level micro current detection system with single channel signal bandwidth less than 100 Hz. To solve this problem, this paper designs a high reliability big data acquisition and storage system based on FPGA and ADS1258 conversion[3]. In this design, FPGA is used as the main control chip, and through FPGA cache technology, 16 channels of data collected by sensors are fused and stored in Flash in real time.

2. System Architecture Design

The whole device consists of two parts: acquisition and storage, including a data recorder and an editor. The editor mainly collects data in the working process, including 16 channels of data collected by sensors and command data sent by FPGA, and sends the received data to the data recorder after a series of processing including caching, framing and packaging. The data recorder

mainly stores and records the data transmitted by the editor, and sends the data when the PC sends and receives the data request. The overall frame structure is shown in Fig.1. During the experiment, the signals collected by the sensor include 6 environmental noise signals and 10 impact signals[4]. The voltage range of these two analog signals is between 0 and 5 V. ADS1258 analog-to-digital conversion chip is selected for analog signal conversion. ADS1258 conversion chip, with a range of 0 to 5 V, supports 16 sampling channels, with a sampling frequency of 23.7KS/s and a 24-bit accuracy, can collect data in automatic scanning mode, which meets the design requirements. The working flow of the system is as follows: (1) After the switch instruction is isolated and filtered by optocoupler, the analog signal is collected. (2) Sixteen analog signals collected by the sensor are isolated from high-frequency noise signals by linear optocoupler. (3) The signal after linear isolation is transmitted to ADS1258 analog-to-digital conversion chip for A/D conversion. (4) The data signal is stored in the FPGA buffer. Complete the framing and packing of FPGA data. (5) The packaged data is stored in the memory card. (6) The collected data is analyzed and transmitted to the PC for display through the network cable readback channel[5].

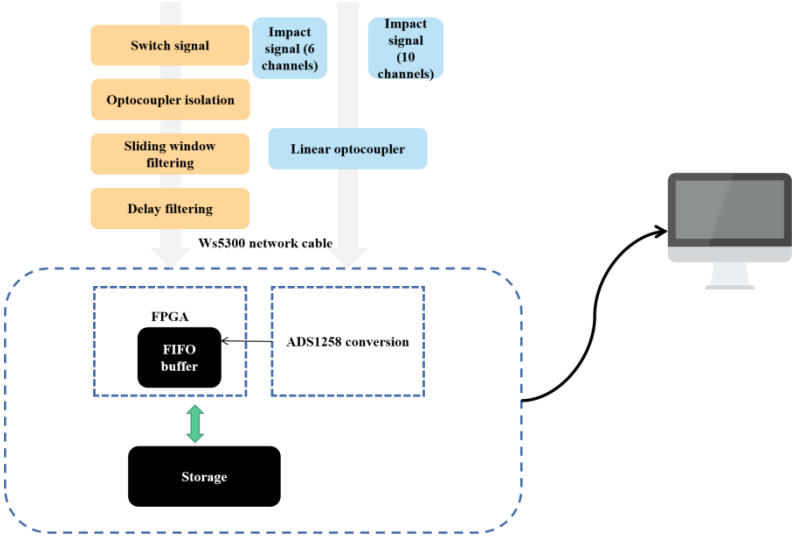

Figure 1: Block Diagram of Overall Structure

3. Hardware Design

3.1 Design of Interference Signal Isolation Circuit

When the analog signal is collected by the sensor, there are high-voltage interference signals, which will cause the circuit components to be damaged. Therefore, before the sensor data signal is transmitted to the A/D converter, a design scheme is needed to isolate and filter the high-voltage interference signals. Usually, the transformer is used for high-level signal isolation, which makes the transformer have a large inductance value, resulting in the bulky design of the acquisition device. The acquisition device designed in this paper adopts photoelectric coupling isolator for high-level filtering.

3.2 Design of Analog-to-Digital Conversion Circuit

ADS1258, a high-precision chip, is used as the conversion chip, which has high conversion accuracy, fast conversion frequency and more conversion channels, and can realize flexible configuration of sampling frequency. The three power supply parts of ADS1258 chip are:

(1) The analog part AVDD is powered by 0 ~ 5V, and AVSS is connected to the analog ground;

(2) The digital part is connected to FPGA, DVDD is connected to 3.3V, and DGND is connected to digital ground;

(3) Reference voltage:VREF=VREFP-VREFN, because the stability of the reference voltage is related to the accuracy of the data collected by the chip, the 5V voltage generated by the high-precision voltage-stabilizing chip AD586 is used as the reference voltage input, with the accuracy of 2mV and low noise drift.

The CLKSELclock pin is externally connected with a 3.3V voltage signal. The CLKIO pin is the input of the 16MHz clock signal generated by the FPGA control chip. The AD_DOUT, AD_CS, AD_SCLK and AD_DIN pins are connected to the FPGA chip through 22Ω exclusion to configure their internal registers AD_RESET, AD_START, AD_PWDN and AD_DRDY pins are also connected to the FPGA control chip through exclusion to control the conversion, reset, start-up, low power consumption setting and data conversion of ADS1258. Operational amplifiers are connected between UXOUTP and MUXOUTN, ADCINP and ADCINN to control the delay time of the internal converter, so as to ensure that when switching to a new channel, the new conversion has not started to have enough time interval[6].

4. Software Design

4.1 Design of Analog Signal Data Framing Structure

In this experiment, 16 channels of data were sampled, including 10 impact signals (A1 ~ A10), a single channel sampling rate of 8kHz, and 6 noise signals (B1 ~ B6), with a single channel sampling rate of 16kHz and a total data sampling rate of 176kHz. In order to achieve uniform sampling of signals, it is necessary to ensure the uniform time interval of the same signal sampling point in one frame of data, so it is necessary to design a uniform framing structure for analog signals. The noise signal of 16kHz is placed at the beginning of the data frame structure. In order to save space, 11kHz is set as the sampling rate of each sampling point in a frame of data, and the highest sampling frequency is 16 times[7]. Therefore, each noise signal in a frame of data needs to appear 16 times, that is, 16 sampling points, so that the data frame structure has 16 lines. Total sampling rate of data is 176kHz, and the sampling rate of each line is 176/16=11kHz. The number of sampling points in each line is 11/1=11kHz. At the same time, it is necessary to add a frame end flag and a frame count signal at the end of each frame, so as to detect whether there is frame loss or frame error in the data acquisition process. Set the number of columns in the preliminary frame structure to 13 columns. The data frame is a 16×13 matrix, with a total of 208 sampling points, of which the frame mark is 16 sampling points and the frame count is 16 sampling points. According to the designed framing structure, the total sampling frequency of the matrix becomes 208kHz. The final data framing structure is shown in Table 1, where C1 ~ C16 are frame flag bits and D1 ~ D16 are frame count bits.

Table 1: Data Framing Structure

line	row												
	1	2	3	4	5	6	7	8	9	10	11	12	13
1	A_1	A_2	A_3	A_4	A_5	A_6	B_1	B_2	B_3	B_4	B_5	B_6	B_7
2	A_1	A_2	A_3	A_4	A_5	A_6	B_8	B_9	B_{10}	C_1	C_2	C_1	C_2
...	...	...	...	...	...	...	...	...	...	...	...	...	...
15	A_1	A_2	A_3	A_4	A_5	A_6	B_1	B_2	B_3	B_4	B_5	B_6	B_7
16	A_1	A_2	A_3	A_4	A_5	A_6	B_8	B_9	B_{10}	C_{15}	C_{16}	C_{15}	C_{16}

Each sampling point in Table 1 is sampled at 1kHz, and the total sampling frequency becomes 208kHz. For A1 sampling point, the interval within a frame of data is 3 sampling points, and the sampling rate is 208/13=16kHz. It meets the requirement of sampling frequency of noise signal[8].

4.2 Design of Switch Instruction

(1) Logic design of combination switch command

There are three switch command signals in this design, which are system reset, data acquisition and stop acquisition command. Usually, the smaller the percentage of valid commands to the number of encodable commands, the stronger the anti-interference ability of command signals and the higher the reliability of the system. In this paper, three command lines are designed to encode the switch command signal. Eight coded commands can be obtained by three command lines, and the effective commands account for 37.5% of the total coded commands. The performance of the combined coding meets the design requirements. The specific design command signal codes are shown in Table 2. Through the coding design of the combined switch command, the conversion between any switch command needs to change two signals. When one signal is disturbed, the other two will be similarly disturbed. If the acquisition data command 101 is changed to 111 after being disturbed, only one channel of signal will be changed. Because 111 is an invalid coding command, the influence of the interference signal is eliminated.

Table 2: Switch Instruction Coding Table

Condition	Cmd3	Cmd2	Cmd1
System reset	1	0	0
Collecting data	1	0	0
Stop acquisition	0	0	1

(2) Filter the switch command.

In the process of hardware design, the optical coupling filter is designed to filter the switch command signal initially, but there are two kinds of interference in the actual environment, one is high-frequency electromagnetic interference signal, which usually accounts for 10% of the effective data bits, and the other is long-term noise signal caused by jitter. In this paper, the switching control signal is further filtered by setting up a software filtering method combining sampling voting with delay filtering. Firstly, the high-frequency noise interference is eliminated by sampling voting[9]. In this paper, the effective signal experiment environment is designed to maintain about 2100ns, each instruction bit is 700ns, and the interactive window width is 77.8ns, that is, one instruction bit is sampled 9 times continuously, and when the collected effective level is more than 4 times, it is considered as an effective instruction bit. Sampling voting method can filter out high-frequency noise, but it can't get good results for long-time jitter noise signals. Based on sampling voting method, this paper designs a delay filter to eliminate jitter, and continuously samples the switch command signal at high frequency to obtain N sampling points. If the N sampling values are the same, the command signal is considered to be valid; otherwise, the interference signal exists, so the command state remains unchanged, and the acquisition of N sampling points is restarted. According to the experimental statistics, this paper sets n to 5, and continuously collects 5 points to judge the validity of the instruction[10].

5. Conclusion

In this paper, FPGA is used as the control chip, ADS1258 is used as the analog-to-digital conversion chip to design the acquisition system, FIFO is used as the buffer device, and the switch control is designed to accurately send control commands, which can accurately acquire analog signals with different frequencies. The design makes up for the lack of stability of signal acquisition in the current data acquisition control field. In the high-speed development of regional modules, it is of great practical value and meets the actual test requirements.

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