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Implementation of a Circuit for Precise Time Stamping of Synchronous Message

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Abstract: Highly required by distributed network operation, the clock synchronization technology is very important. The transmit time of synchronization packets should be stamped precisely in a clock synchronization system. Time stamping in the physical layer is necessary to obtain the time precisely. This paper introduces a general precision time stamping circuit based on 10Mb/s and 100Mb/s transmission. The circuit is designed and manufactured in 0.18μm CMOS technology supporting Precise Timing Protocol based on IEEE 1588. The circuit is verified by an experimental system. The test results show that the general precision time stamping circuit can mark the stamps for UDP/IPv4 Ethernet format in the physical layer. The circuit has an ability to mark a time stamp in less than 60μs.

1. Introduction

IEEE 1588 clock synchronization protocol has got a lot of attention in aerospace, Internet of things and other fields with popularization of distributed network[1,2]. Based on IEEE 1588 protocol, the Precision Time Protocol(PTP) has been widely concerned by research institutes and companies for its nanosecond synchronization precision[3]. As stipulated in the PTP, the slave clock obtains the network delay and the deviation between the master and slave clock by transmitting a synchronization message. Then the slave clock should be adjusted to implement time synchronization[4]. However, the accuracy of obtained network delay and deviation are depended on the precision of the timestamp, which is determined by the position of the timestamp transmitted on[5].

Figure 1 shows the typical time stamping process of IEEE 1588 protocol. Owing to the uncertainty of the protocol stack delay and the network transmission, the accuracy of clock synchronization will be in the unit of seconds. As a result, it is necessary to generate the timestamp in the physical layer[6,7]. Based on 10BASE-T ,100BASE-TX and IEEE 1588 PTP protocol, a general precision time stamping circuit is introduced in this paper.

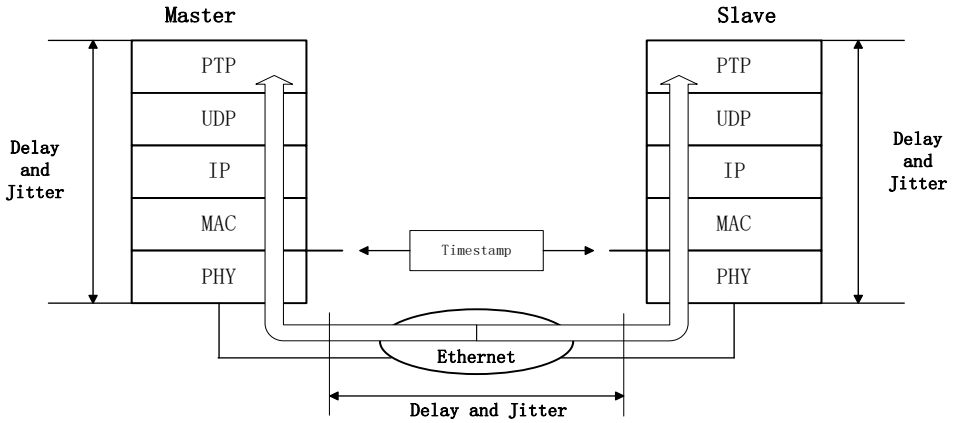


Figure 1: The typical time stamping process of IEEE 1588 protocol

2. Timestamp Marking Method

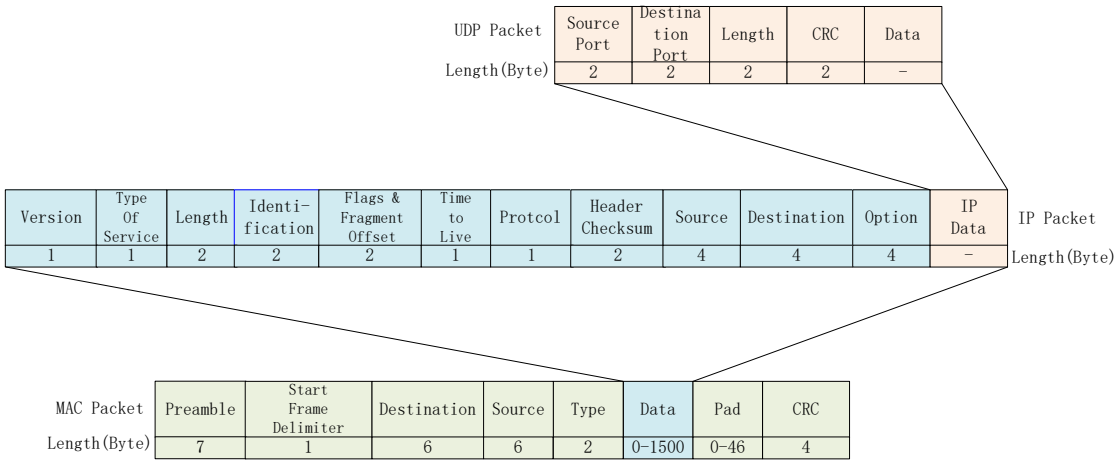


Figure 2: The Packet encapsulation format of UDP/IP message

Generally, an IEEE 1588 PTP message is encoded in UDP(User Datagram Protocol)/IP(Internet Protocol) encapsulation. The encapsulation format is shown in Figure 2. A message packet consists of preamble code, start frame delimiter(SFD), destination address, source address, data length, message data, filler character and CRC(Cyclic Redundancy Check) checksum. Except for data and filler character, the length of other parts is fixed. Besides, message data is consisted of IP message header and IP message data which is built of UDP message header and UDP message data. The length from preamble code to UDP message header is fixed, the circuit design is based on this.

The time when the SFD ended is the arriving or leaving time of synchronization packet, according to the IEEE 1588 protocol. This time is the timestamp, which will be saved in timestamp register when an PTP message has been captured by the physical layer chip. The circuit designed in this paper captures the arriving or leaving time of SFD, and records the fields at specific locations, The recorded fields, such as Ethernet type, IP message type, etc., are compared with default values to decide if they are identical, and the messages passing the filtering would be identified as PTP messages[8].

3. Precision Time Stamping Circuit Design and Verification

3.1. Precision Time Stamping Circuit Design

The circuit structure designed in this paper is illustrated in Figure 3. The Transmit module. Receive module, Management Register are not concernment of this paper, and the design is typical[9]. The IEEE 1588 Clock Synchronization Circuit is composed of Transmit Mark module, Receiving Mark module, Transmit and Receive Message Processing module, Management Register, Interrupt Control and IEEE 1588 Clock module. The Transmitting Mark module has the ability to detect the sending of IEEE 1588 messages. Then the time when the message has arrived is recorded and stored in Transmit Mark register. The Transmit Message Processing module analyses the message. If the message is correct, an interrupt would be generated to inform the upper application to obtain the timestamp by reading the Management Register. The function of the Receive modules is similar to the Transmit modules, and to avoid repetition, it is not described in this article.

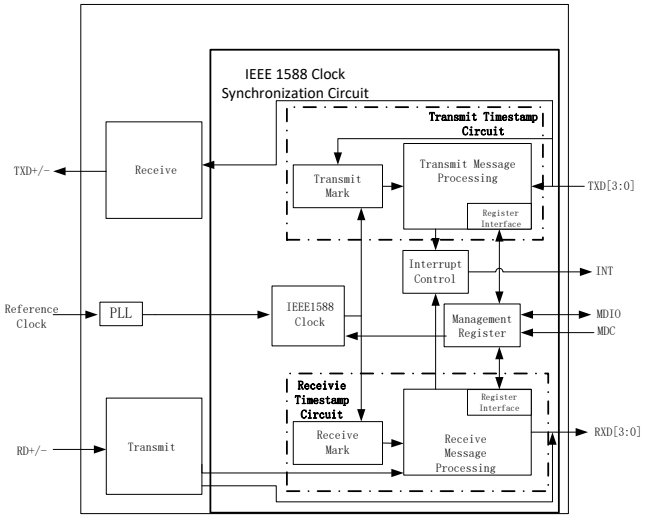
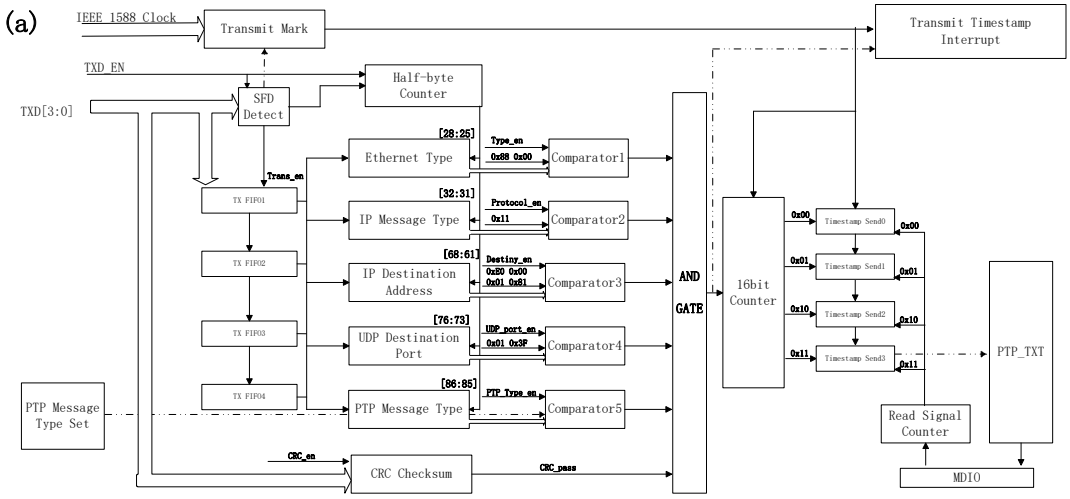
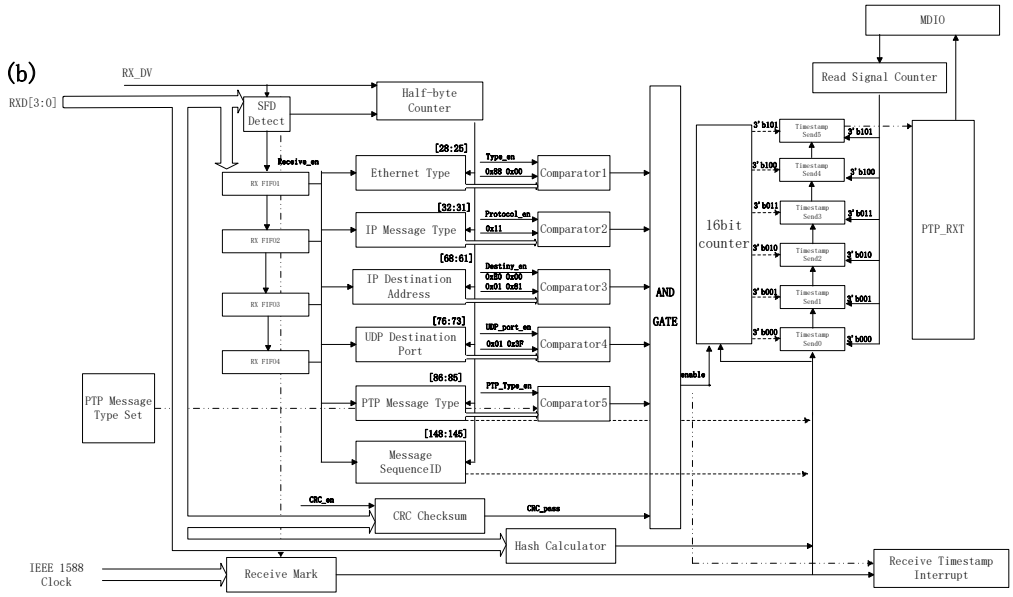


Figure 3: The architecture of the circuit



(a)Schematic of Transmit Timestamp Circuit



(b)Schematic of Receive Timestamp Circuit

Figure 4: (a) Schematic of Transmit Timestamp Circuit (b) Schematic of Receive Timestamp Circuit

To illustrate the timestamp circuit clearly, the schematics of Transmit and Receive Timestamp Circuit are shown in Figure 4. Figure 4(a) shows the schematic of Transmit Timestamp Circuit. The Transmit Timestamp Circuit is consisted of four TX FIFOs(First Input First Output) to store the transmit data for filtering, one SFD Detect module which detects the SFD in the transmit data, one Transmit Mark register which stores the time when the data arriving, one Half-byte Counter used for field registers to extract fields, five field registers(Ethernet Type, IP Message Type, IP Destination Address, UDP Destination Port and PTP Message Type) used for different fields filtering, five comparators with control pins used for filtering, one CRC Checksum module used for CRC check, four Timestamp Send registers used to store timestamps, one PTP_TXT register used for transmitting the timestamp to MDIO port, 16bit Counter and Read Signal Counter used for storing or reading timestamp data to the registers.

When a TXD[3:0] data arriving at the Transmit Timestamp Circuit, the SFD Detect module would detect if the SFD is in the transmit data, then the Half-byte Counter would begin to count the half-byte number of the transmit data, and the values of IEEE 1588 clock would be stored in the Transmit Mark register. Meanwhile, the field registers store the transmit data when the Half-byte Counter counts to specific numbers. As shown in Figure.4(a), during the accumulation of the counter, when the counted number is identical to the values in the brackets, the data in the TX FIFOs are stored in corresponding registers. For example, if the counted number counts to 25~28, the data in the TX FIFOs are the fields corresponding to the Ethernet type and the value is stored in the Ethernet Type register. By that analogy, the IP message type, IP destination address, UDP destination port and PTP message type are stored in the other field registers.

The values stored in the field registers are compared with the set value to filter the message by the Comparators. Most of the set values are fixed. As shown by Figure. 4(a), 0x08 0x00 means that Ethernet type is IPv4. 0x11 means that IP message type is UDP. 0xE0 0x00 0x01 0x81 means that the IP destination address is 224.0.1.129, which is the default multicast address in the IEEE 1588 protocol. 0x01 0x3F means that the UDP destination port should be 319, which is used to transmit the PTP messages generally. While the PTP message type can be configured by the register. For example, 0x00 means the PTP message type is Sync message. Each comparator can be controlled

by the management register. In addition, the CRC Checksum module can also be used. If the calculated value equals to the CRC message, the CRC_pass signal is generated, indicating that the CRC has been checked.

The TXD[3:0] data that satisfies all filtering conditions is a valid PTP message. When the AND gate outputs a high level signal, the value stored in Transmit Mark register is induced to the Timestamp Sending0, meanwhile the 16bit Counter starts. The Transmit Timestamp Interrupt module generates an interrupt signal to inform the upper application that the PTP_TXT register is available. After reading this register, reading enabling signal counter starts. The value stored in Transmit Mark register is 256 bit (128 bit for nanoseconds and 128 bit for seconds). In fact the four Timestamp Send registers become a 64 bit width, 4 bit depth FIFO, and counters are necessary for timestamps storing and reading.

The structure of Receive Timestamp Circuit is similar to the Transmit Timestamp Circuit, as shown by Figure. 4(b). However, some parts are different. For receiving timestamp, except the nanoseconds and seconds, Hash value, PTP message type and sequenceID are also important to the upper application. As a result, Hash calculator is needed for Hash value calculation, and the Message SequenceID register and PTP Message Type register should be connected with Timestamp Send registers. Besides, the number of Timestamp Send registers is six, for the purpose of storing and transmitting the values of nanoseconds[31:0], seconds[31:0], sequenceID[15:0], message type[3:0] and hash value[11:0].

3.2. Simulation of the Circuit

The circuit is simulated by VCS. Figure.5(a) shows the simulation results of timestamp transmit. The TXD[3:0] data is stored in four TX FIFOs. When the circuit detect the SFD, and the filtering conditions are met, the second and nanosecond timestamps are recorded in the Timestamp Send registers and the interrupt signal(INT) is pulled down. The value of Time_Stamp_s[31:0] is 0x00000001 and the value of Time_Stamp_ns[31:0] is 0x00054150, indicating that the arriving time is 1.00034400s. The timestamps are transmitted through MDIO port. Figure. 5(b) shows the simulation results of the receiving. The process is similar to the transmitting. However, the difference is also obvious that the values of Hash, message type and sequenceID are filtered and transmitted to the PTP_RXT register. The Hash is 0x02B1, PTP message type is 0x00 and sequenceID is 0x0001. The function of the circuit has been verified.

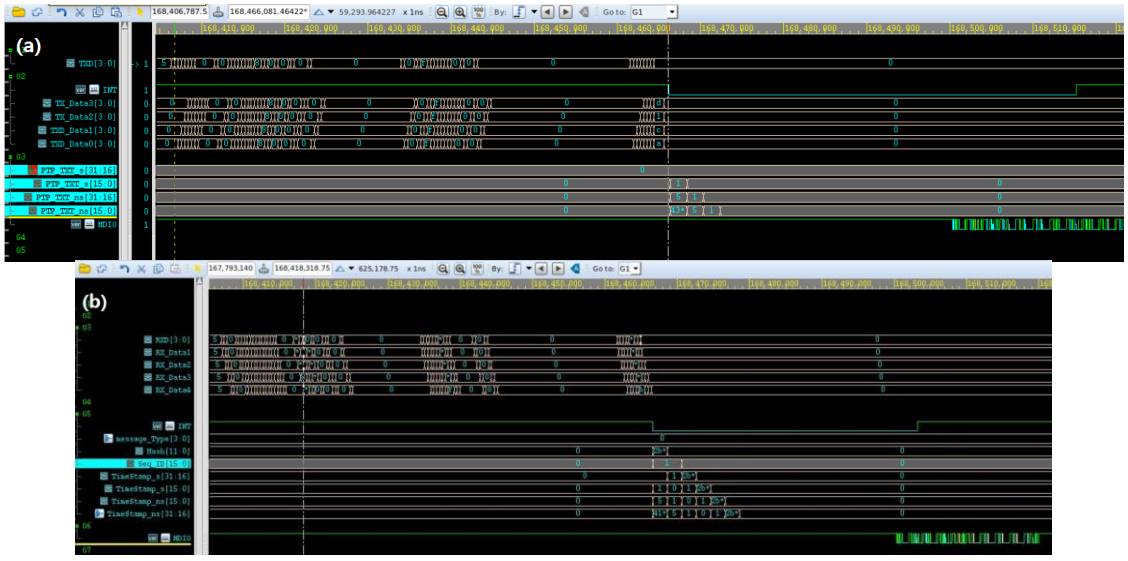


Figure 5: (a) Simulation of timestamp transmitting. (b) Simulation of timestamp receiving

3.3. System Level Verification

After verification, the whole chip is manufactured in 0.18μm CMOS technology. The layout schematic of the chip is shown by Figure 6. The chip can perform 10BASE-T/100BASE-TX transmission with synchronous message accurate timestamp.

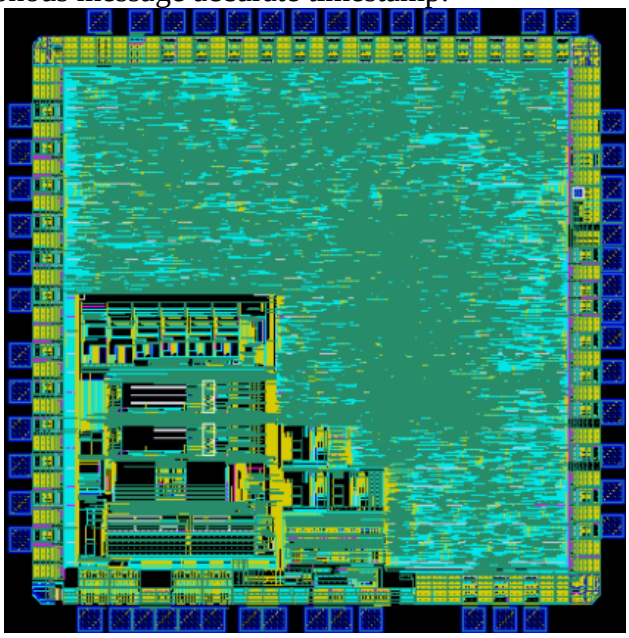


Figure 6: The layout schematic of the chip

System level verification is performed with the FPGA(Field Programmable Gate Array) verification system based on Xilinx K7 as shown in Figure 7. The system consists of a PC(as host computer), a verification PCB and an oscilloscope to detect the signal. The chip is configured to 10BASE-T transmission mode, and the Ethernet PTP message type is configured to 0x00, indicating that only the Sync message is recognized. The timestamp register is read by the PC after the PC receives the interrupt from the chip.

Figure 7: The photo of practice system

The test result is shown in Figure 8. The TXD_0, TXD_1, TXD_2, TXD_3 stand for transmitted data. INT stands for timestamp interrupt. The INT pulled down after the chip detect the SFD(which is 0xD5), and the time interval is 58.852μs, indicating the circuit has an ability to mark the timestamp in less than 60μs. The value of the register read by PC is 0x3390, 0x1688, 0x0010, 0x0000, indicating that when the IEEE 1588 clock reaches 16.378024848s, the chip has outputted the message. This indicates that the function is valid.

Figure 8: The result of board level verification

4. Conclusions

In this article, a general precision time stamping circuit based on 10BASE-T/100BASE-TX protocol is designed and manufactured in 0.18μm CMOS technology. The chip also supports the Precise Timing Protocol based on IEEE 1588. The function of the circuit is verified by simulation and an experimental system. The test results show that the stamping circuit can mark the stamps for UDP/IPv4 Ethernet format in the physical layer and the circuit has an ability to mark the time stamp in less than 60μs.

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