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Study of the square wave response of a first-order RC circuit

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Abstract: The square wave response of a first-order circuit has an oscillatory nature. In this paper, from first giving simulations of first-order circuits with different duty cycles at different frequencies and then eliciting questions and conjectures, the square wave response of different cases is then unified and the response expressions are rigorously derived using mathematics, and the response characteristics are finally discussed and the square wave response characteristics of first-order circuits are named stable oscillations.

1. Introduction

S First-order RC and RL circuits are circuits that contain only one dynamic element. The equations listed for analysing the response of first-order circuits are first-order differential equations and are therefore called first-order circuits[1]. When a square wave signal with different duty cycles at different frequencies is applied to a first order circuit, the capacitor or inductor element will be reciprocally charged and discharged or charged and discharged at the set frequency signal, i.e. the capacitor voltage or inductor current response will obey the exponential law of reciprocal cycles[2].

In this paper, the Multisim simulation environment is used to study how the response of a first-order circuit changes under different frequency square-wave signal sources, and to summarize the laws of change, using formulae to deduce the general expressions for the response of components, combined with simulation experiments to demonstrate the characteristics of the square-wave response of first-order circuits[3].

2. Square wave signal

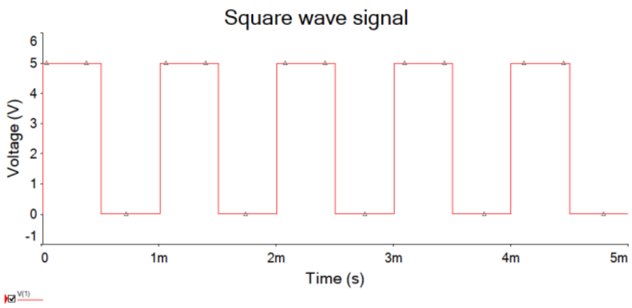

Figure 1 Square wave signal

This experimental square wave signal source will be used with an amplitude of 5V and a duty cycle of D. In the following, we will first study a positive square wave signal with D = 50%, where the frequency is the variable, as Figure 1 shown.

3. Modelling analysis

When studying transient analysis of first-order circuits, most textbooks state that for first-order circuits, if the charge time reaches $3\tau \sim 5\tau$, then the engineering considers the charge to be complete, and similarly if the discharge time reaches $3\tau \sim 5\tau$, then the discharge is also considered complete. This leads to the question of what the waveform of a first order circuit will look like if the charge time does not meet a given criterion, i.e. the charge time is short, and if the discharge time does not meet a given criterion. For this reason, this paper will be analysed through simulation using Multisim.

In order to observe the charging and discharging process of the circuit, a positive square wave signal is applied to the RC or RL circuit so that the time constant τ = 0.001s is used to observe the voltage waveform across the capacitor in the RC circuit and the current waveform in the RL circuit by constantly changing the frequency of the signal source so that the period T* is equal to 0.1τ, 0.5τ, τ, 4τ and 10τ respectively.

Here we use Multisim to set the RC circuit with a resistance of 1.0kΩ and a capacitance of 1.0μF to give a time constant of 0.001s, and the RL circuit with a resistance of 1.0kΩ and a capacitance of 1.0H to give the same time constant of 0.001s.

4. Simulation validation

With the above modelling design, the results are verified by simulation as shown in the following set of figures(Figure 2-Figure 11).

(1) First order RC circuit response

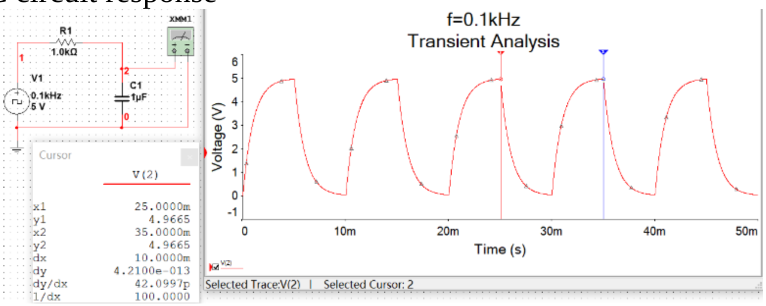

Figure 2 RC circuit signal source frequency of 0.1kHz

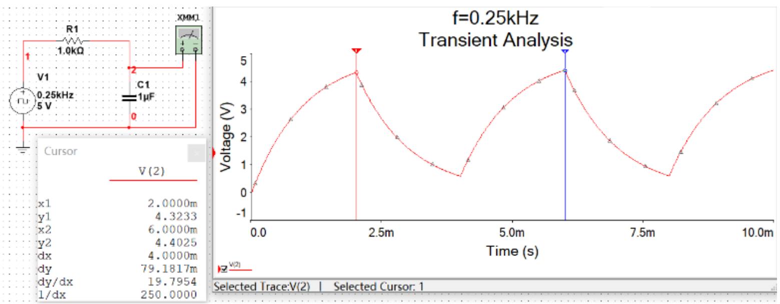

Figure 3 RC circuit signal source frequency of 0.25kHz

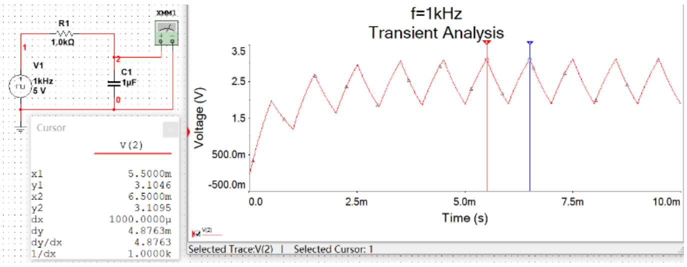

Figure 4 RC path signal source at 1 kHz

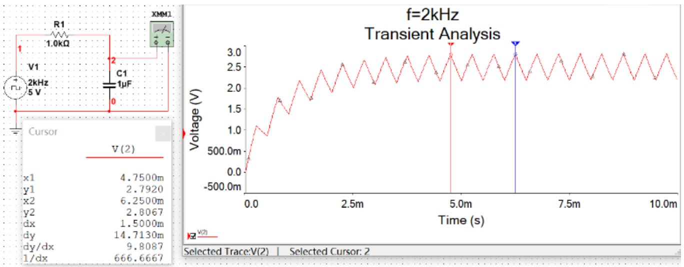

Figure 5 RC circuit signal source at 2kHz

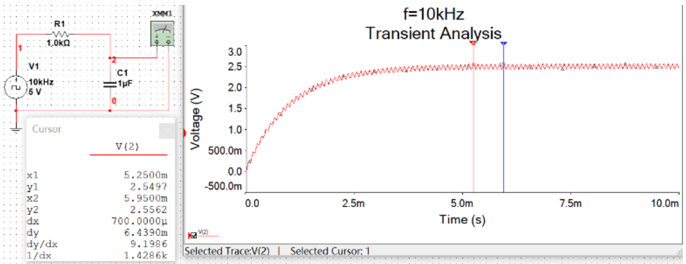

Figure 6 RC circuit signal source at 10 kHz

(2) First order RL circuit response

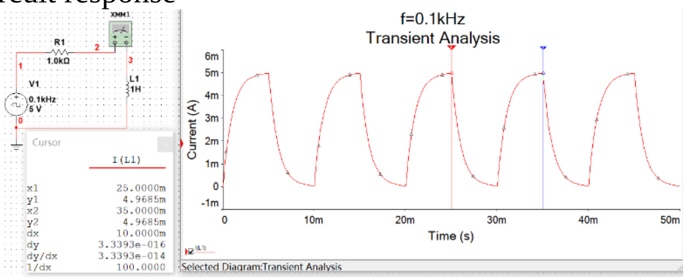

Figure 7 RL circuit signal source frequency of 0.1kHz

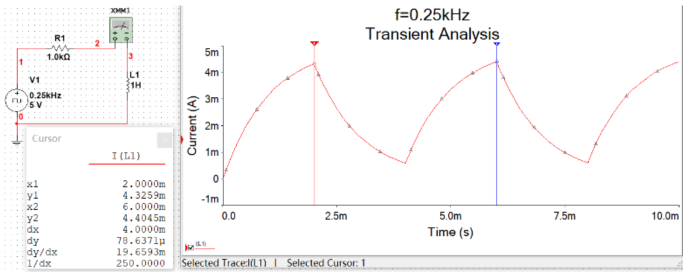

Figure 8 RL circuit signal source frequency of 0.25kHz

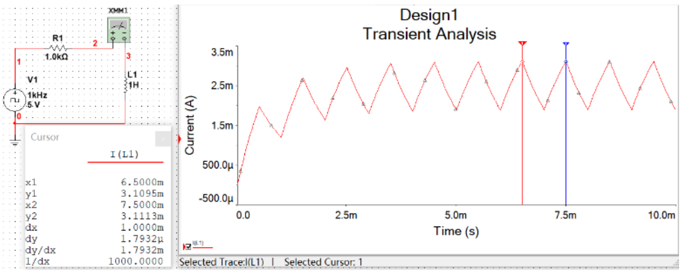

Figure 9 RL circuit signal source at 1kHz

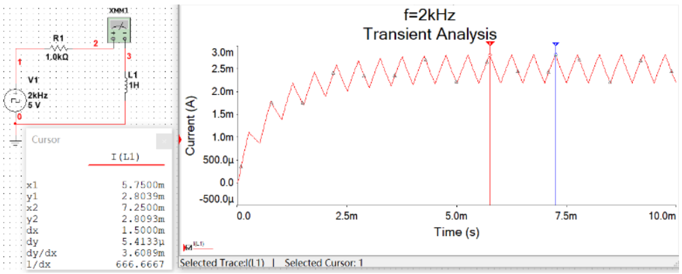

Figure 10 RL circuit signal source at 2kHz

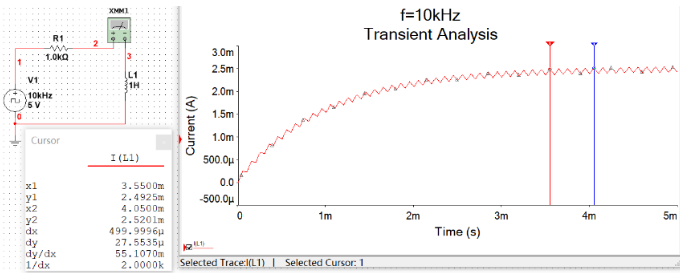

Figure 11 RL circuit signal source at 10 kHz

5. Discussion and reflection

Me For the sake of brevity in the derivation of the final equation below, the periods we talk about below refer to the half-period of a square wave, i.e. $T = \frac{1}{2}T^*$.

It is simple to see intuitively that when the period is much greater than the time constant τ , the circuit is considered to be fully charged and discharged in engineering terms, but when the cursor is moved in the simulation to see the magnitude, it is clear that the circuit is not fully charged and discharged in the true sense of the word, i.e. it does not reach the steady state value, because the true sense of the steady state value of charging and discharging is when it is always charging under the action of a DC signal source or discharging without a signal source This is because the true steady state value of charging and discharging is the value at which time tends to infinity when the circuit has been charged by a DC source or discharged without a source[4].

When the period T is proportional to the time constant τ, the voltage value of the capacitor in the RC circuit ends up charging and discharging in an interval, and the current value in the RL circuit also remains in an interval, which can be described as a "stable oscillation".

If the period T is much smaller than the time constant τ, the voltage value of the capacitor in the RC circuit and the current value in the RL circuit will tend to stabilise in a straight line, but on closer analysis this is very similar to the above situation and is also a "stable oscillation". However, the interval of oscillation is significantly smaller.

In fact, for a period T much larger than the time constant τ, it can also be called "stable oscillation", except that this interval is infinitely closer to its stable value at the charge/discharge steady state. Therefore, we can see all three cases as charging and discharging not being truly stable, but with different amplitude intervals, some being very close to the steady state value and therefore considered to be fully charged and discharged within the error allowed. Some "stable oscillation" intervals are better observed, while some "stable oscillation" intervals are so small that the waveform can be considered as a straight line, and what is the approximate value of this straight line?

The upper limit of the "stable oscillation" of the voltage across the capacitor is U_{on}. Assuming that the circuit has been charged and discharged for an infinite number of cycles, it starts to reach its upper limit at U_{on} from its lower limit at U_{down} after one cycle at T. The applied supply voltage is U_s, so using the three-element method for first-order circuits, the expression for the circuit after one cycle is:

$$U_{on} = U_S + (U_{down} - U_S)e^{-\frac{T}{t}} \tag{1}$$

Similarly, the voltage across the capacitor goes from its upper limit at U_{on} to its lower limit at U_{down} after another cycle at T. Using the three-element method, we can obtain the expression for the capacitor at

$$U_{\text{down}} = 0 + (U_{\text{on}} - 0)\ \mathrm{e}^{-\frac{T}{\tau}} \tag{2}$$

Combining these two expressions gives,

$$U_{\text{down}} = U_{\text{on}}\mathrm{e}^{-\frac{T}{\tau}} = \frac{U_S \mathrm{e}^{-\frac{T}{\tau}}}{1 + e^{-\frac{T}{\tau}}} \& U_{\text{on}} = \frac{U_S}{1 + \mathrm{e}^{-\frac{T}{\tau}}} \tag{3}$$

After deriving these two expressions we discuss the following case. For a period T much larger than the time constant τ, the upper and lower limits can be approximated as $U_{down}= 0$, $U_{on}= U_s$ respectively, which is consistent with our simulation and analysis results. When the period T is not very different from the time constant τ, there is an appreciable interval between U_{on}, U_{down}. When the time constant T is much smaller than the time constant τ, then the expression above can be used to approximate $U_{\text{on}} = U_{\text{down}} = \frac{U_S}{2}$. As the frequency increases and the period decreases, the difference between the upper and lower limits of this "stable oscillation" decreases, and the amplitude of the square wave with the maximum upper and lower limits decreases, eventually the difference between the upper and lower limits becomes 0 when the frequency is high enough, i.e. a straight line as described above.

Also the square wave response of the RL circuit will have a similar pattern to that of the RC circuit, so I won't go into that here.

What if the duty cycle D is greater than 0 and less than 1 but not equal to 50%? This means that the charging time and the discharging time of the circuit are not equal in one cycle T*. For example, if the charge time is greater than the discharge time, or if the charge time is less than the discharge time, will the "stable oscillation" situation described above still occur? Again, we present the simulation results below before analysing the causes. Here we control the frequency of the power supply at 1kHz and vary its duty cycle D by 5%, 20%, 40%, 60%, 80% and 95% to observe the voltage waveform across the capacitor(Figure 12-Figure 17).

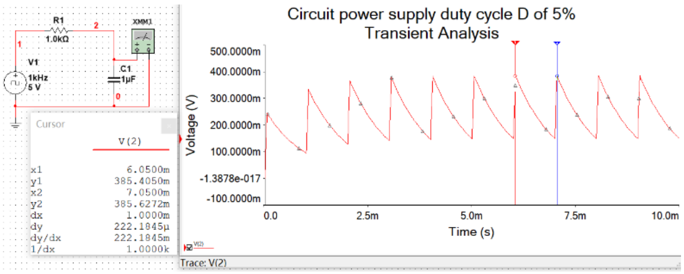

Figure 12 Circuit power supply duty cycle D of 5%

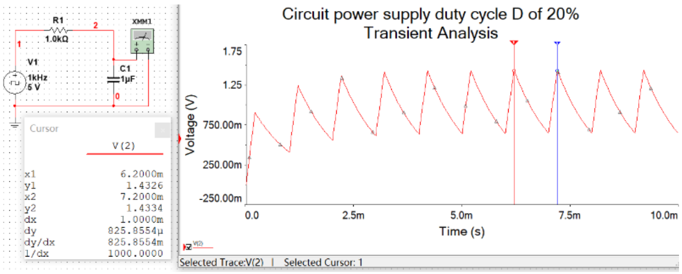

Figure 13 Circuit power supply duty cycle D of 20%

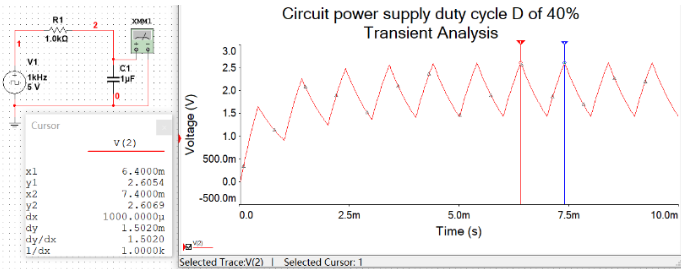

Figure 14 Circuit power supply duty cycle D of 40%

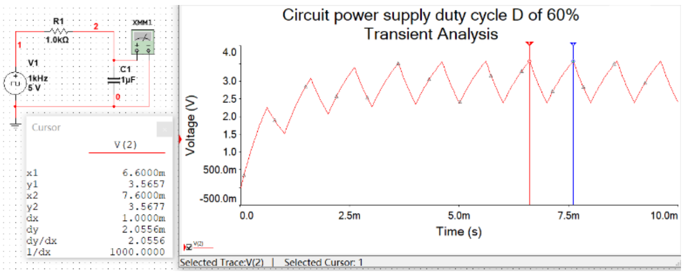

Figure 15 Circuit power supply duty cycle D of 60%

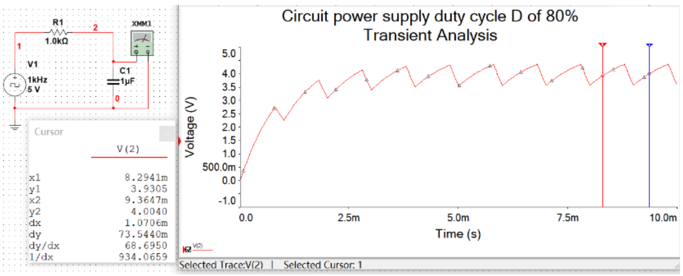

Figure 16 Circuit power supply duty cycle D of 80%

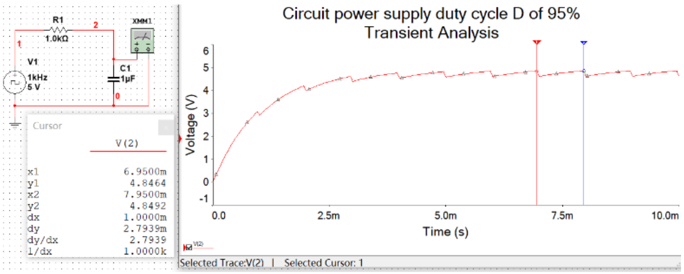

Figure 17 Circuit power supply duty cycle D of 95%

From the above simulation results it is clear that the circuit is characterised by "stable oscillations" at the same period (frequency unchanged) and at different charge and discharge times. In the following, we will first give a strict mathematical derivation and then explain the reasons for this characteristic[5].

The period we use here is expressed as the entire period of the square wave *T**, its charging time is *DT** and its discharging time is(1-*D*)*T**. Using the three-element method of circuit response, we get

Charging.

$$U_{\text{on}} = U_S + (U_{\text{down}} - U_S)\mathrm{e}^{\frac{-DT^*}{\tau}} \tag{4}$$

Discharge.

$$U_{\text{down}} = 0 + (U_{\text{on}} - 0)\,\mathrm{e}^{\frac{-(1-D)\,T^*}{\tau}} \tag{5}$$

Solution.

$$U_{\text{on}} = \frac{1-\mathrm{e}^{\frac{-DT^*}{\tau}}}{1-\mathrm{e}^{\frac{-T^*}{\tau}}}U_S \;\&\; U_{\text{down}} = \frac{\mathrm{e}^{\frac{-(1-D)\,T^*}{\tau}} - \mathrm{e}^{\frac{-T^*}{\tau}}}{1-\mathrm{e}^{\frac{-T^*}{\tau}}}U_S \tag{6}$$

Obviously in the duty cycle *D* is greater than 0 less than 1, even if not equal to 50% there will be an upper and lower limit, when *D* is equal to 1, bring in the expression $U_{\text{on}} = U_{\text{down}} = U_s$. This is easy to understand because when the duty cycle is 1, it is a DC source and the voltage across the capacitor is the amplitude of the DC source when the circuit is steady-state; similarly when the duty cycle is 0, then $U_{\text{on}} = U_{\text{down}} = 0$, it is clear that a duty cycle of 0 means that there has been no input, the power supply is short-circuited, the capacitor has not been charged and its voltage is naturally 0. Adjusting the frequency of the power supply means changing its period, so the above expression contains the three parameters of a square wave Duty cycle, frequency, amplitude, and the time constant of the circuit.

Below we have a simple visualisation of why there are still "stable oscillations". See Figure 15, Figure 16 and Figure 17. It can be seen that a duty cycle of more than 50 per cent, i.e. a charge time greater than a discharge time, is equivalent to a more-gentle charging waveform in the Figure 18. This ensures that the voltage rises and falls at the same value for more charging time and less discharging time. Similarly, with a duty cycle of less than 50 percent, with less charging time and more discharging time, the Figure 18 Only a steeper section of the charging waveform and a smoother section of the discharging waveform can be matched.

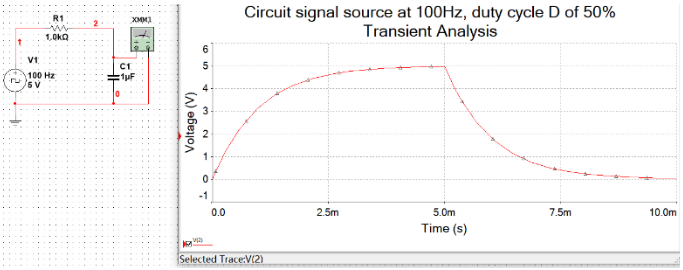

Figure 18 Circuit signal source at 100Hz, duty cycle D of 50%

Similar we can make the period T^* in the above expression tend to zero (which is very small compared to the time constant τ), both equations are then of type 0:0 and we find the limit of the equation $U_{\text{on}} = U_{\text{down}} = DU_S$, which only relates to the duty cycle and amplitude of the square wave and not to the time constant τ. We take the Fourier decomposition of the square wave with duty cycle D and amplitude U_S and obtain its DC component, i.e. its average value, which is also DU_S. In this way, we do not know the duty cycle of a square wave, and design an RC circuit with suitable parameters to make its time constant τ larger, so that we can, under a relatively high frequency square wave signal, note that at this time, after many charging and discharging processes, the voltage waveform across the capacitor is approximately a straight line, we can just use a multimeter DC gear to measure its value, and then the square wave amplitude is known, we can The duty cycle is roughly obtained. Figure 19 The current waveform of the RL current (resistor voltage waveform) will have similar characteristics, so we will not repeat them here.

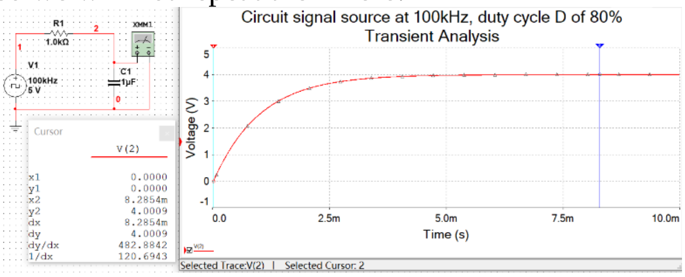

Figure 19 Circuit signal source at 100kHz, duty cycle D of 80%

In summary, as long as a first-order circuit square wave response exists, there will be a process of "stable oscillation".

References

[1] Zhao Qiang, Sun Dianping, Zhang Wenqian, Guo Chaoxiu. Parsimonious analysis of the first-order RC response under square wave excitation[J]. University Physics, 2020, 39(04):34-36.

[2] Zhang Wei, Ye Yanqun, Xing Liang. A brief discussion on the response of RC circuits under square wave excitation[J]. Journal of Electrical and Electronic Teaching, 2015, 37(03):60-62.

[3] Li Caiping, Li Lesheng. Study of first-order RC circuit response under square wave excitation[J]. Digital Technology and Applications, 2011(11):106-108.

[4] Huang Chung, Yang Yao, Cai Qiufeng, Xiang Dan. Research on frequency response characteristics of RC-based circuits in teaching [J]. Electronic Technology and Software Engineering, 2021(15):59-61.

[5] Jia Yanyan, Deng Yuyuan, Cui Jingna. RC first-order circuit zero-input response teaching method in one lesson[J]. Electronic World, 2016(16):25+27.