Design of data acquisition and transmission system for BOTDA

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Abstract: According to the demand of BOTDA optical fibre sensor for real-time application, a high-speed data acquisition system with graphical operation interface is designed by using FPGA and USB. In this paper, hardware architecture and logic design are carried out for data acquisition with FPGA as the control device, and the upper computer with functions of data display and graphic demonstration is designed by using C# language on the PC terminal. Finally, joint debugging is carried out for the lower computer and the upper computer, and the experimental results show that the high-speed data acquisition and transmission functions are successfully realized, which meets the design requirements of the data acquisition system in BOTDA optical fibre sensor.

1. Introduction

Brillouin optical time domain analysis (BOTDA), as a distributed optical fibre temperature and strain sensing technology, has the advantages of long sensing distance, high spatial resolution and high measurement accuracy in temperature and strain detection [1-3]. With the rapid development of optical fibre sensor technology in recent years, BOTDA distributed optical fibre sensor attract a large number of scholars to research and is gradually applied to various fields such as border security, and structure health monitoring [4-6]. At present, theoretical research on Brillouin optical fibre sensor technology is basically mature, and more researchers have invested in optical fibre sensor measurement to improve the performance of the system. For example, in 1995, Bao etc. used BOTDA to realize the temperature measurement with sensing distance of 51 km, spatial resolution of 10m for the first time [7]. In order to improve the spatial resolution of BOTDA system, Dominguez-Lopez etc. adopted differential pulse pair (DPP) to realize the spatial resolution of 1cm on 10km fibre [8].

Distributed optical fibre sensing technology based on BOTDA have made great progress, but the engineering application of distributed optical fibre sensor is still stay in the laboratory stage. The reason is that the detection of temperature and strain variation in traditional BOTDA system is done offline. Usually, offline data acquisition card is used to collect sensor data, and then the data is handed over to DSP for processing. Obviously, this kind of detection method cannot fully meet the needs of practical application.

To make the BOTDA system practical, real-time data acquisition and transmission of high-speed Brillouin data is a key point that needs to be solved. Therefore, this paper proposed a design of high-speed data acquisition and transmission system based on Field Programmable Gate Array (FPGA) for BOTDA.

2. System Design and Implementation

2.1. Overall System Design

The overall design of the system can be divided according to different functional modules, which are mainly divided into two parts: signal collection and data transmission. The overall framework of the system is shown in Figure 1. Analog signal conditioning circuit is used for analog input signal amplitude modulation and filtering. Analog to Digital Converter (ADC) is used to convert analog signal into digital signal. FPGA, as the processing unit of proposed system, is mainly responsible for data processing, caching and transmission, etc. USB data transmission module is used to transmit data. The upper computer is written in Visual Studio with C# language, mainly realizing the functions of connecting devices, displaying data and waveform, and saving files. Power supply and reset circuit provide power supply and reset control for the whole system, which is critical to the whole system. FPGA controls the ADC to collect sensing data, and then sends the data to the FIFO (First in, First out) of USB and transmits the data to the upper computer for display, storage and other processing.
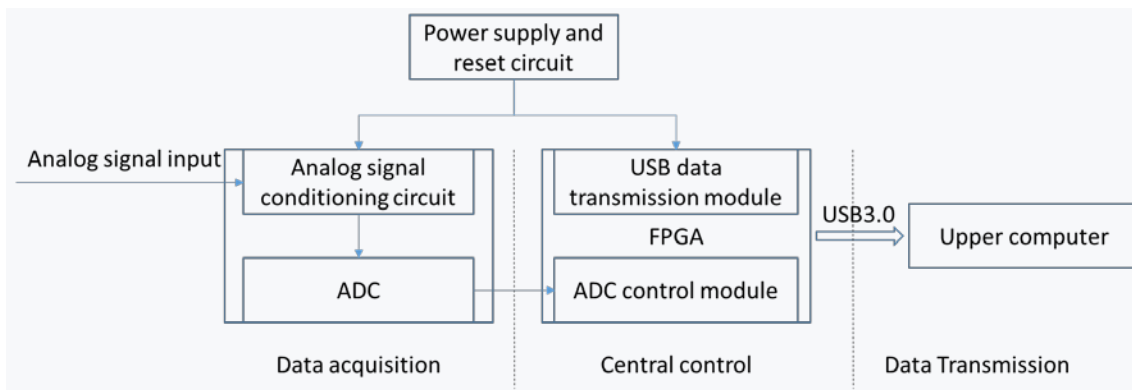

Figure 1: Overall framework of the proposed system.

2.2. Data Acquisition Module

The logic design of data acquisition module is shown in Figure 2. To complete the process of data acquisition, the input sensing data from ADC needs to go through the dynamic phase adjustment (DPA) sub-module, serial-parallel conversion sub-module (realized by LVDS) and data format adjustment sub-module successively. The DPA sub-module is used to realize phase compensation for clock and data of LVDS sub-module to achieve the purpose of correct reception. After the data has been processed by LVDS, the data should be adjusted to a suitable format for the post processing or transmission.
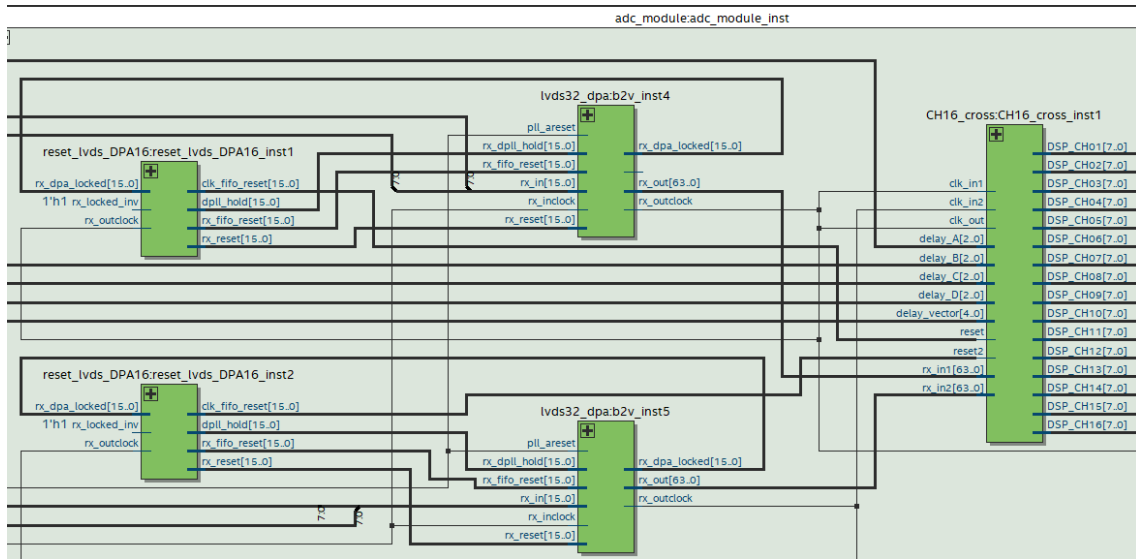
Figure 2: RTL viewer of data acquisition module.

The main idea of DPA is to make the input data be collected at the most suitable time through the phase adjustment function of phase-locked loop (PLL). Firstly, PLL is used to generate a number of clocks with different phases. Secondly, the data collection is triggered at the effective edge of each clock to compare which clocks can capture the stable and accurate data. Lastly, in a series of clocks with different phases that meet the sampling conditions, the middle clock is selected as the sampling clock to make the system has the maximum timing margin and the reliability of the interface is guaranteed.

2.3. Data Transmission Module

The logical hierarchy design of data transmission module is shown in Figure 3, which mainly includes three parts: (a) USB configuration module, (b) command processing module and (c) data operation module. Before the process of data transmission, USB input ports and output ports should be configured firstly by USB configuration module. Here, we set EP2 as output ports and EP6 as input ports, each port containing two FIFO of 1024 bytes respectively. In addition, the USB transmission mode is set as block transmission mode, which transfers 1024 bytes of data at one time. The USB command processing module mainly processes the commands from the PC upper computer and carries out corresponding processing according to the commands sent by the PC upper computer. The communication protocol of proposed system is defined as follows: when receiving the command word of 0X01, start the data collection and transmission function; when receiving the command word of 0X10, stop the above process. The data operation module mainly completes the reading and writing of USB according to the corresponding timing sequence of USB chip.
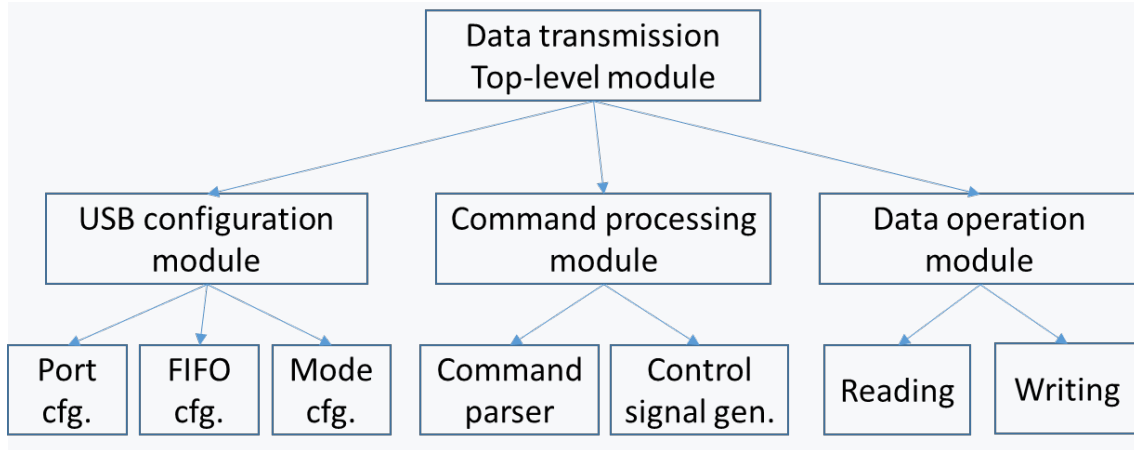
Figure 3: Logical hierarchy design of data transmission module.

The asynchronous write data state transition diagram of USB is shown in Figure 4 (a). Firstly, EP6 was set as communication port in the idle state with address selection line FIFOADDR0 was set to 1 and FIFOADDR1 was set to 0. When receiving write data command, status flag was set to high (busy), then enter from idle state to write command state; in the write command state, in order to ensure that SLWR signal can have a descending edge, SLWR is first pulled up, then is pulled down after two clock cycles, so that the direction of the data bus is changed to output. After eight clock cycles, SLWR is pulled up again, the data is stored in FIFO, and the data is write done, then the state enter from write data state to write done state. In the write done state, the status flag is pulled down (idle) after four clock cycles, state enter into the idle state, and complete a write data operation. The asynchronous read data state transition diagram is similar to write data state transition diagram, as shown in Figure 4 (b), which is not detailed here.
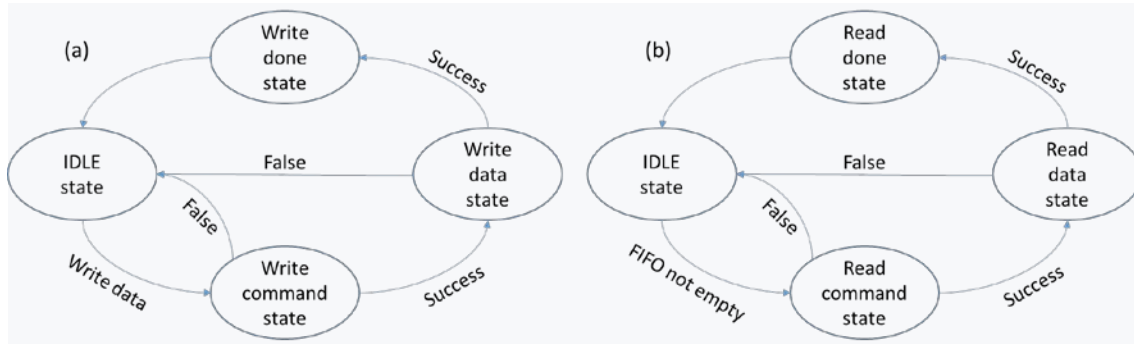

Figure 4: State transition diagram of data operation module, (a) Write data and (b) Read data.

3.   Experimental setup and result

To verify the correctness of proposed system, signals with different waveforms and frequencies are generated by the function generator and input into the ADC module. For results demonstration, an upper computer is designed with functions of USB connection, send, receive, stop, clear, save files, data display and drawing demonstration etc. The experimental results are shown in Figure 5, it can be seen that whether the sine wave data (Figure 5(a)), square wave data (Figure 5(b)), rectangular wave data (Figure 5(c)) or saw tooth wave data (Figure 5(d)) can be received and be recovered

correctly. The small deformations observed in Figure 5 is induced by the low Signal Noise Ratio (SNR) of ADC and the curves are not drawn in smooth mode in upper computer.
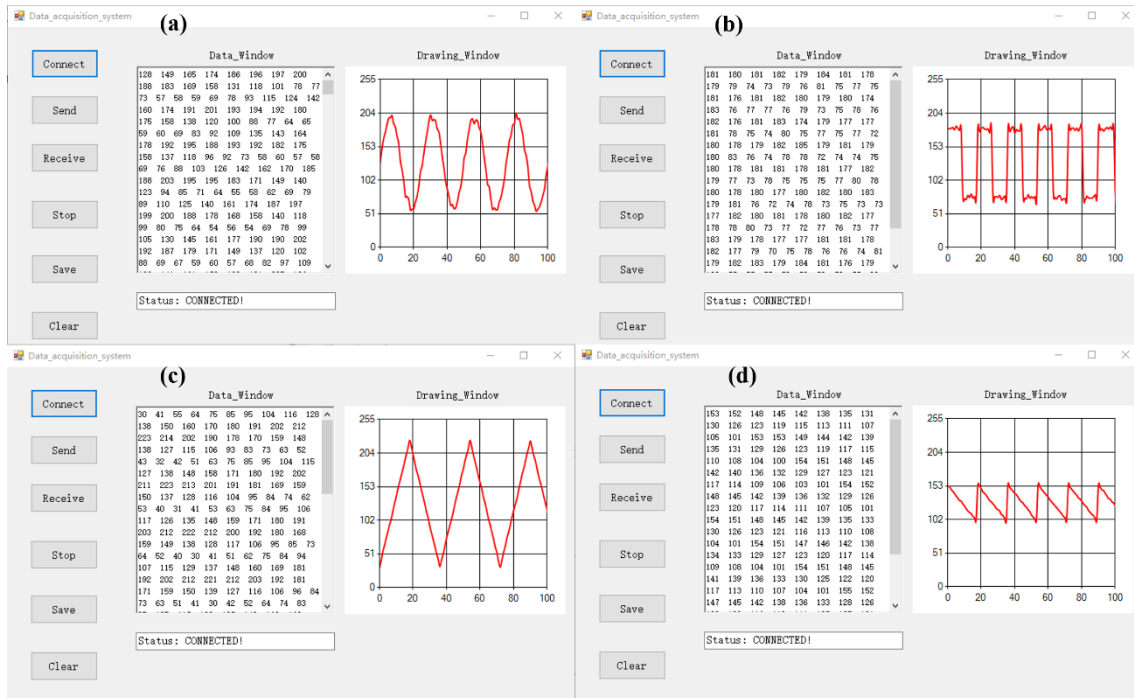

Figure 5: Experimental result of proposed data acquisition system.

4. Conclusions

The dynamic measurement system based on BOTDA optical fibre sensor has a very broad application prospect and has become the focus of researchers. Based on BOTDA optical fibre sensor system, this paper designs a high-speed data acquisition and transmission system, which has the advantages of fast transmission rate and intuitive and dynamic data display. The proposed system can solve the deficiencies of current BOTDA system which using general data acquisition card.

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