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Research and Design of ETC System's Key Technologies Based on FPGA

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Abstract: This paper not only describes the design of a central overhead ETC lane and the lane controller, canceling the traditional Lane rail to achieve a transparent ETC to the user, but also effectively solves problems of congestion. And by optimizing the internal structure of the ETC baseband circuit, this paper uses the FPGA technology to achieve the international standard of B baseband codec - Manchester codec.

1. Introduction

Compared with the traditional manual charging method, ETC system reduces the manual transaction link, the vehicle through the toll station time greatly reduced. However, the ETC system also has some shortcomings. Such as the current lane detection sensor equipment accuracy is not high, there is misidentification of the situation; if the deduction is not successful, easily lead to congestion and so on.

In this paper, by analyzing the current situation of ETC system, the ETC lane of automatic railings is demonstrated, and the key modules and baseband codecs in ETC system baseband circuits are realized by using FPGA technology with rich logic resources and high real-time advantages. An M-sequence verifies the correctness of the design.

2. ETC System Design

In the ETC system, the most important is the on-board equipment (OBE) and roadside unit (RSE), both in the ETC signal transmission, processing plays a decisive role[4]. In general, the functions of the vehicle equipment include signal transmission, signal processing, account management, identification card read and write functions, in which the signal transmission and processing by the baseband circuit. The function of the road side unit mainly includes signal transmission, processing, and signal modulation and demodulation transceiver, the signal transmission processing also rely on the baseband circuit to complete. Both the on-board device and the roadside unit baseband circuits contain two important blocks of High-level Data Link Control (HDLC) and baseband codecs.

(a) Realization of Lane Controller Based on FPGA

It can be seen that the excitation source is the state of the vehicle in the lane controller. The signal that can be recognized by the system is whether the OBE and RSE communication are successful and whether the lane controller can fully identify the vehicle label and whether the system can deduct the cost. These three conditions determine the signal indication of the lane aids. Designed based on Verilog HDL hardware programming language, the above three conditions as input to the signal signal of each device as an output.

This is the result by using Quartus II 8.0. According to the simulation chart, we can see that the lane controller can be used to control all kinds of lanes.

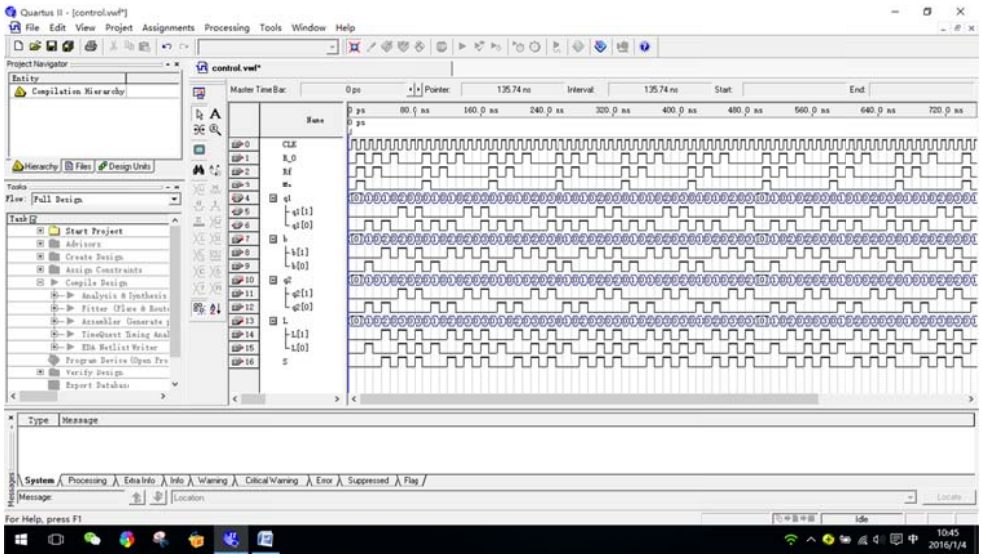

Fig.1 The controller emulates the waveform

3. HDLC Design and Related Module Implementation

As a bit-oriented protocol, HDLC (Advanced Data Link Control) protocol can achieve non-coding, high reliability and efficient transparent transmission. Especially for high-speed synchronous half-duplex and full-duplex data communication, so in the ETC system signal transmission, it is widely used as a standard.

(a) HDLC internal structure

According to ETC system baseband circuit and advanced data link control protocol frame structure, can be analyzed HDLC mainly includes the receiver and the sender two parts, the role of the sender is the first from the CPU data stream stored in the register, and then the register data Serial and parallel conversion, through the state machine to construct the protocol frame structure, and generate the CRC code, and then the stream into the "0" operation, the standard frame format after the transmission to the baseband circuit coding module. And the receiver is the reverse process of the sender.

(b) Implementation of HDLC Protocol in FPGA

Since the data stream flows internally, it is serially converted by the corresponding device before the state machine is controlled. Regardless of how to control the state machine, and ultimately the need for HDLC protocol within the various modules to achieve the processing of data, the following describes the key modules within the agreement FPGA implementation and design.

(c) Verification and Simulation of HDLC Protocol Controller

Since the main function of the advanced data link control protocol is to send the constructed frame and receive the post-resolution frame structure. This paper does not involve the physical layer data transmission, therefore, in the simulation, the sender and the receiver together to test whether the sender structure frame structure is successful, and whether the receiver can correctly analyze the original data. Figure 2 shows the simulation waveform of the protocol controller transmitter. Figure 3 shows the simulation waveform of the receiver of the protocol controller. From the two pictures can be seen, the sender and receiver data is consistent, proved that the design is reliable.

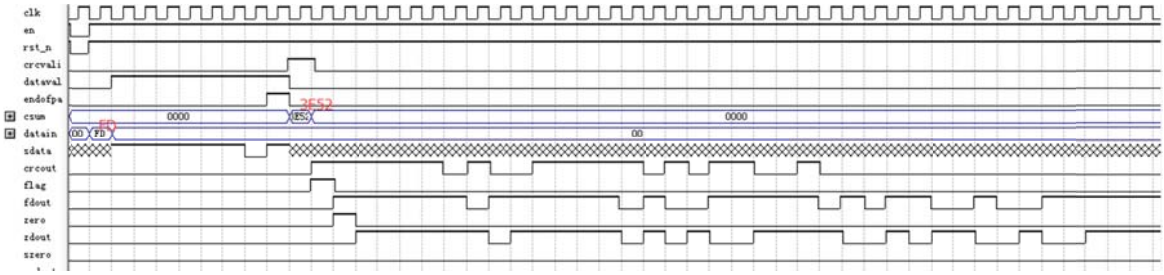

Fig.2 Protocol controller transmitting end simulation waveform

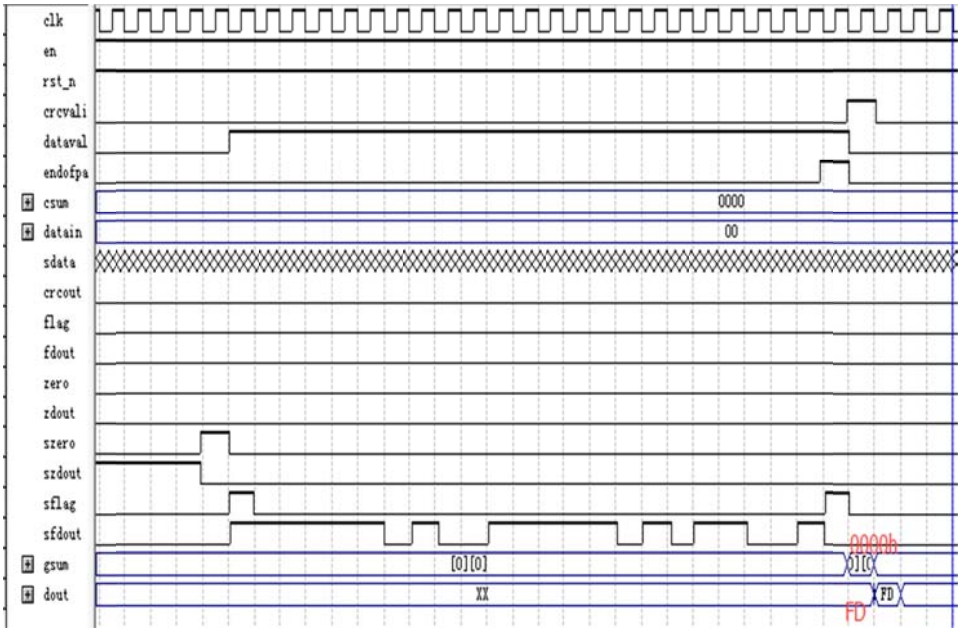

Fig.3 Protocol controller receiver simulation waveform

4. Baseband Codec

In this design, we divide the design of the encoder into three modules, in which the pseudo-random sequence generator module generates the M-random sequence that needs to be encoded, and the divider module divides the system clock to obtain the required clock frequency for Manchester coding , The Manchester encoding module encodes the M random sequence and outputs the encoded result.

(a) Functional simulation

The correctness is still tested here using send-receive verification. The transmitter of the baseband circuit sends four sets of parallel data, "1010111", "10111111", "00000000" and "00000000". The ModelSim simulation of the transmitter is shown in Figure 4.

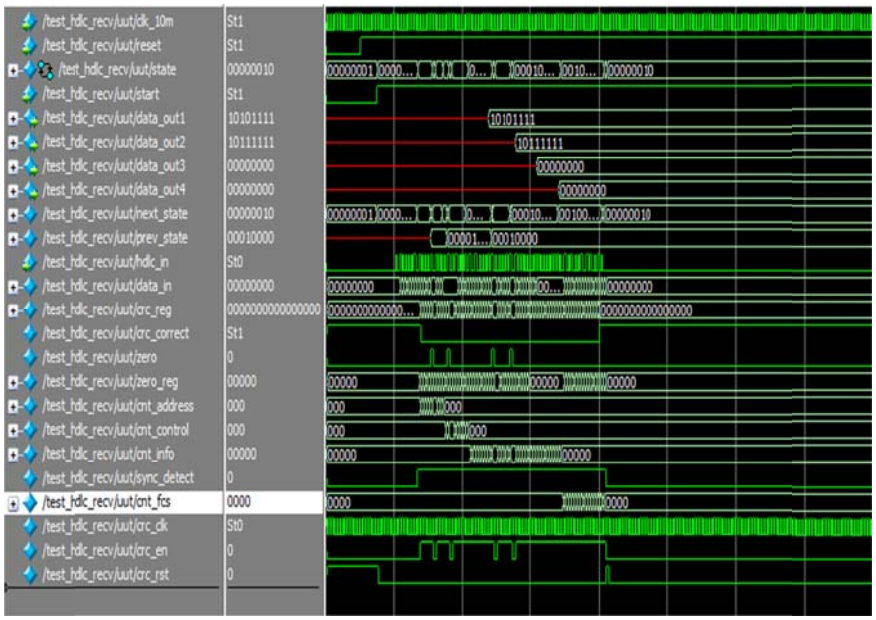

Fig.4 Simulation of transmitter side of baseband circuit

Figure 5 for the receiver of the simulation map, we can see that the receiver received the sender sent the four groups of data, and CRC check to 0, indicating that the data transmission process is not an error, the baseband circuit design is correct.

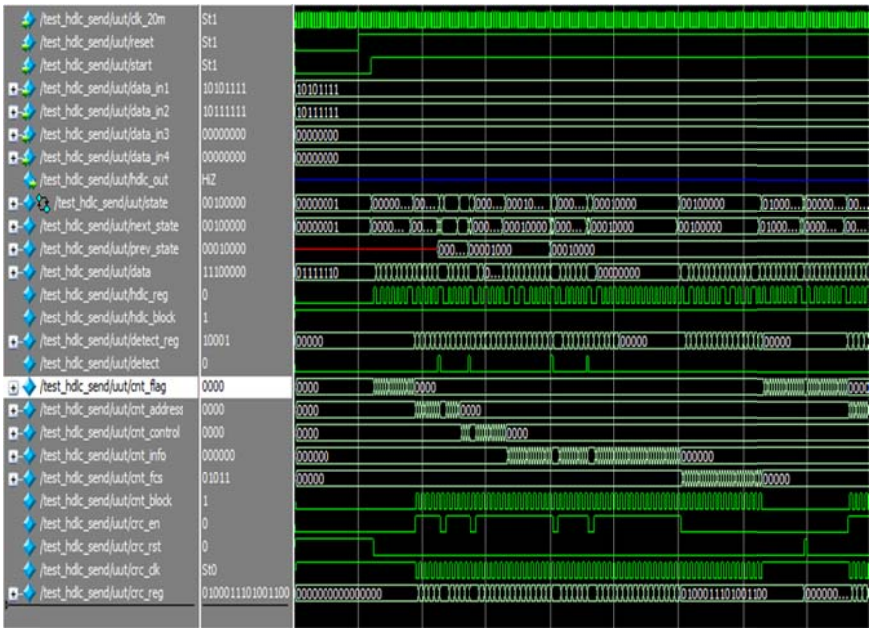

Fig.5 Simulation of Receiving End of Baseband Circuit

5. Summary

In this paper, the ETC lane without automatic railings design can greatly improve the traffic rate of the vehicle. The key modules and baseband codecs of ETC system baseband circuits are realized by using FPGA technology with rich logic resources and high real-time advantages. The correctness of the design is verified by an M-sequence, which is of reference significance to the further improvement of ETC system, and it has certain application prospect and high practical value.

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